



Indy® R1000 Reader Chip (IPJ-P1000)

Electrical, Mechanical, & Thermal Specification

The Impinj® UHF Gen 2 RFID product line includes the Indy® R1000 reader chip based on award-winning technology acquired from Intel Corporation. This highly integrated reader chip and supporting software deliver the key building blocks for a full range of UHF Gen 2 RFID readers.

Indy® R1000 Reader Chip Overview

| | |
|-----------------------------------|---|
| Air Interface Protocol | EPCglobal UHF Class 1 Gen 2 / ISO 18000-6C <ul style="list-style-type: none">• DSB, SSB, and PR-ASK transmit modulation modes• Dense reader mode (DRM) |
| Integrated Power Amplifier | Configurable. External power amplifier supported for high performance applications |
| Modem | Configurable digital baseband |
| Operating Frequencies | 840–960 MHz |
| Package | 56-pin 8 mm ² QFN |
| Power | Advanced Power Management |
| Process | 0.18 µm SiGe BiCMOS |
| RSSI | Configurable |
| Sensitivity | -95 dBm (DRM) -110 dBm (LBT) |
| Supported Regions | US, Canada, and other regions following US FCC Part 15 regulations Europe and other regions following ETSI EN 302 208 with & without LBT regulations China, India, Japan, Korea, Malaysia, and Taiwan |

For technical support, visit the Impinj support portal at: support.impinj.com

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1 Introduction

Impinj®'s Indy® R1000 reader chip is a highly integrated, high-performance, low power, SiGe BiCMOS device for ISO18000-6C and Electronic Product Council (EPC) Gen 2 applications. The Indy R1000 reader chip supports a zero intermediate frequency (ZIF) architecture in the worldwide UHF industrial, science, and medical (ISM) band. The Indy R1000 reader chip comprises all of the RF blocks to interrogate and receive data from compatible RFID tags, specifically:

- High compression point quadrature downconverting mixer
- Fully integrated voltage controlled oscillator (VCO)
- Variable receiver (RX) gain control
- Integrated Power Amplifier (PA)
- Integrated RF envelope detectors for forward and reverse power sense
- Integrated multipurpose Analog-to-Digital Converts (ADCs) and Digital-to-Analog Converters (DACs)
- Configurable digital baseband
- High speed synchronous serial bus or 4-bit parallel bus control

When used in the Indy R1000 Development Platform, which includes an example protocol processor and radio control implementation, the result is a fully functional UHF RFID reader.

1.1 Terminology

Table 1: Terminology

| Term | Description |
|---------|--|
| ADC | Analog-to-Digital Converter |
| AGC | Automatic Gain Control |
| AM | Amplitude Modulation |
| ASK | Amplitude Shift Keying |
| AUX | Auxiliary |
| BPF | Bandpass Filter |
| Class 0 | Tags and readers conforming to MIT Auto-ID Center, Class 0 RFID Tag Protocol Specification |
| CORDIC | COordinate Rotation DIgital Computer |
| CW | Continuous Wave |
| DAC | Digital-to-Analog Converter |
| DFT | Discrete Fourier Transform |
| DSB | Double Sideband |
| EOT | End of Transfer |
| EPC | Electronic Product Council |

| Term | Description |
|----------|---|
| FCC | Federal Communications Commission (US Regulatory Body) |
| FIFO | First In, First Out |
| FIR | Finite Impulse Response |
| I | In-phase |
| IF | Intermediate Frequency |
| IIR | Infinite Impulse Response |
| I-Q | In-phase Quadrature |
| ISM | Industrial, Science, and Medical |
| ISO | International Standards Organization |
| ISO18000 | Tags and readers conforming to ISO/IEC FDIS 18000-6:2003(E) |
| LBT | Listen Before Talk |
| LFSR | Linear Feedback Shift Registers |
| LNA | Low Noise Amplifier |
| LO | Local Oscillator |
| LUT | Lookup Table |
| MSB | Most Significant Bit |
| NCO | Numerically Controlled Oscillator |
| PA | Power Amplifier |
| PLL | Phase Locked Loop |
| PoE | Power over Ethernet |
| PR | Phase Reversal |
| Q | Quadrature-phase |
| RF | Radio Frequency |
| RFID | Radio Frequency Identification |
| RSSI | Received Signal Strength Indicator |
| RX | Receiver |
| SSB | Single Sideband |
| TBD | To Be Determined |
| TX | Transmitter |
| TCXO | Temperature Compensated Crystal Oscillator |
| UHF | Ultra High Frequency |
| VCO | Voltage Controlled Oscillator |



1.2 Reference Documents

The Indy R1000 reader chip is fully compliant with the protocol specifications provided in [Table 2](#), as well as with the local regulations in [Table 3](#).

Table 2: Protocol Specification Documents

| Document | Document Number |
|---------------------------|--------------------------|
| ISO/IEC FDIS 18000-6:2005 | Version 2.0, August 2004 |

Table 3: Local Regulation Documents

| Document | Document Number |
|---------------------------|-----------------|
| FCC 47 CFR Ch. 1, part 15 | 10-1-98 Edition |
| ETSI EN 302 208-1 | V1.1.1 |

2 About this Document

This document constitutes the electrical, mechanical, and thermal specifications for the Indy R1000 reader chip. It contains a functional overview, mechanical data, package signal locations, and targeted electrical specifications.

2.1 Indy R1000 Reader Chip Diagrams

A top level block diagram of the analog parts of the Indy R1000 reader chip is shown in [Figure 1](#). The architecture is based on direct conversion for both the transmitter and receiver. A block diagram for the digital parts is shown in [Figure 2](#), and a sample application for the Indy R1000 reader chip is illustrated in [Figure 3](#).

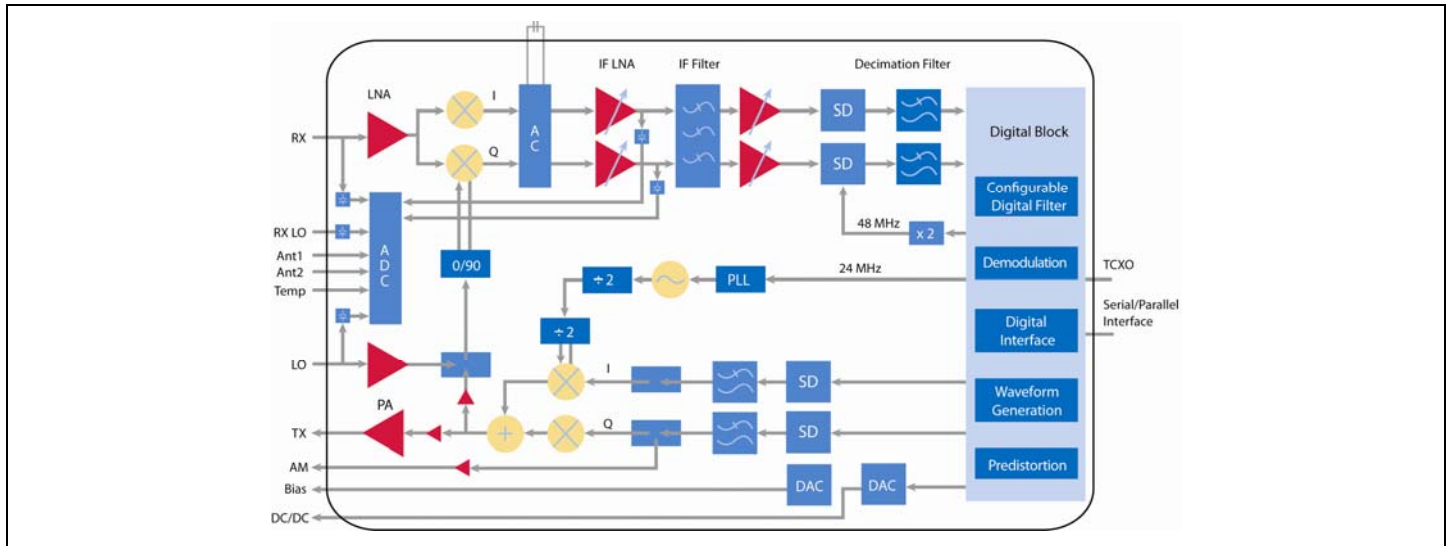


Figure 1: Indy R1000 Reader Chip Top Level RF Block Diagram

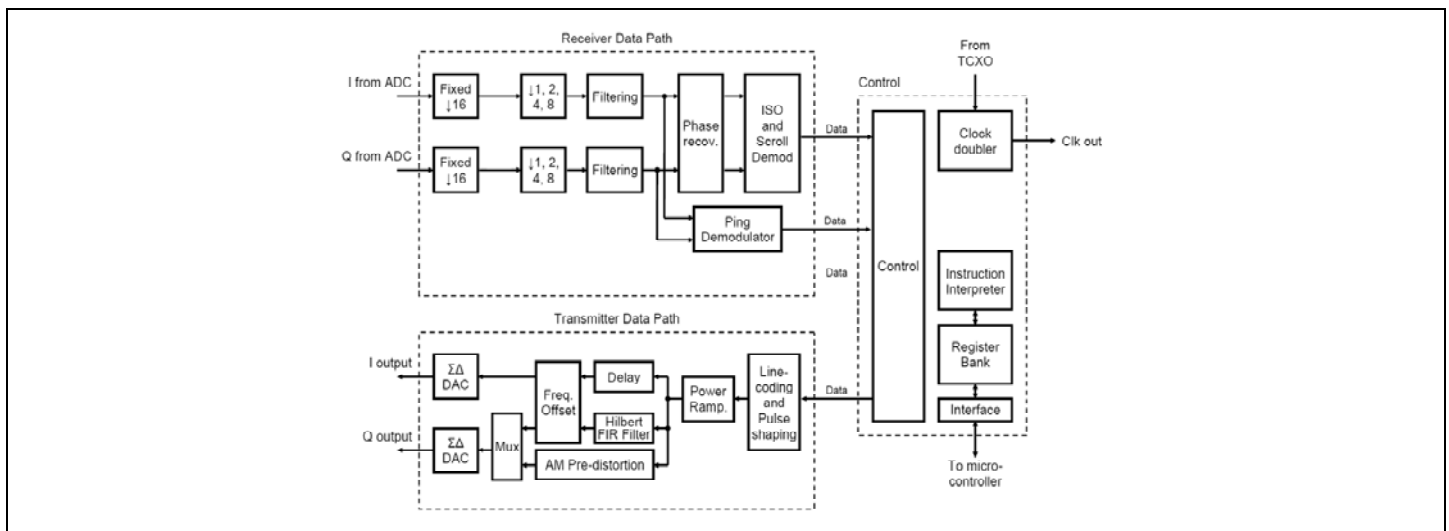


Figure 2: Indy R1000 Reader Chip Top Level Digital Block Diagram

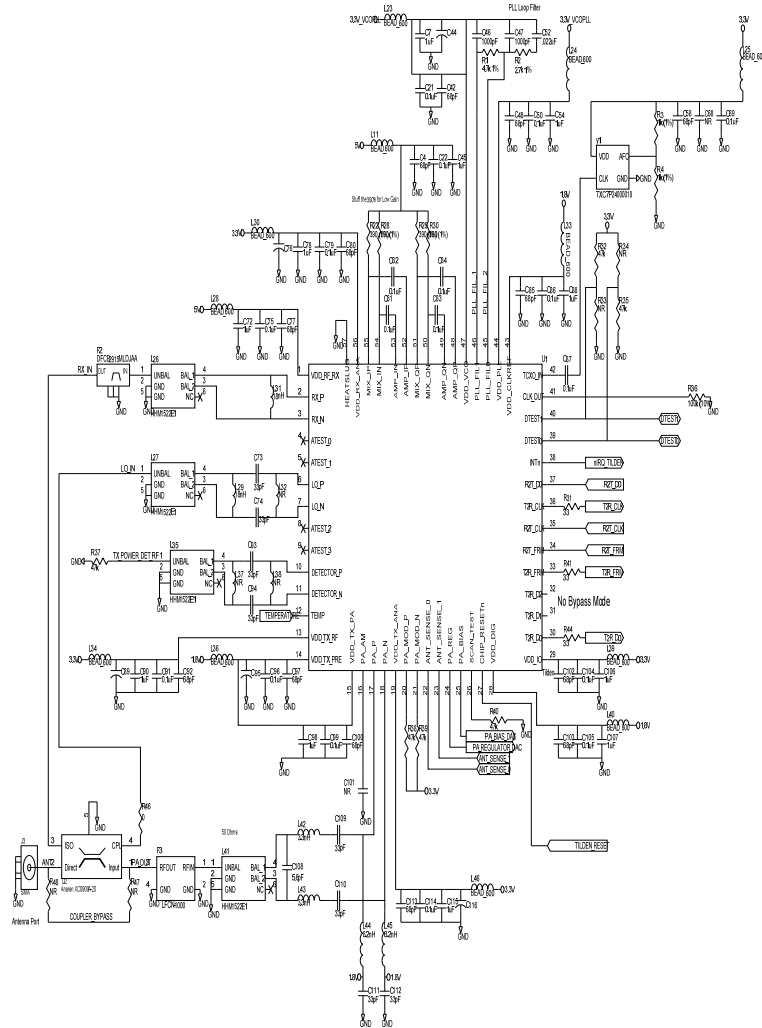


Figure 3: Indy R1000 Reader Chip Sample Application

3 Pin Listing/Signal Definitions

Table 4: Pin Listing and Signal Definitions

| Pin # | Pin Name | Type ⁺ | Description |
|----------------------|---|-----------------------------|--|
| 1 | Vdd_rx_rf | 5.0 V | Supply for receive RF |
| 2 3 | RX_p RX_n | RF In | Differential receive RF input |
| 4 5 | Atest0 Atest1 | A | Analog test bus |
| 6 7 | LO_p LO_n | RF In | Differential RF input from a high impedance tap on transmit path |
| 8 9 | Atest2 Atest3 | A | Analog test bus |
| 10 11 | Detector_p Detector_n | RF In | Differential peak detector input |
| 12 | Temp | A In | Voltage input from a temperature sensor (General Purpose ADC) |
| 13 | Vdd_tx_rf | 3.3 V | Supply for transmit RF, except for PA |
| 14 | Vdd_tx_pre | 1.8 V | PA pre-driver supply |
| 15 | Vdd_tx_pa | 1.8 V | PA supply |
| 16 | Reserved | | Reserved for Future Use |
| 17 18 | PA_p PA_n | RF Out | Differential TX output for all modes |
| 19 | Vdd_tx_ana | 3.3 V | Supply for transmit analog |
| 20 21 | PA_modp PA_modn | A Out | Differential output voltage of PA modulator DAC to apply AM to the PA |
| 22 23 | Ant_sense0 Ant_sense1 | A In | General Purpose ADCs |
| 24 | PA_reg | A Out | General Purpose 8-bit DAC. Can be used to control external PA regulators. |
| 25 | PA_bias | A Out | General Purpose 8-bit DAC. Can be used to control external PA bias. |
| 26 | | D In | Manufacturing Test Pin |
| 27 | Chip_resetrn | D In | |
| 28 | Vdd_dig | 1.8 V | Digital supply |
| 29 | Vdd_io | 3.3 V | I/O supplies |
| 30 31 32 33 | DA0/T2R_DAT[0] DA1/T2R_DAT[1] DA2/T2R_DAT[2] DA3/T2R_FRM | D Bi (slew rate limited) | Bidirectional data interface, multiplexed with SSP T2R frame and data signals, Power-up state: HiZ |
| 34 | ALE / R2T_FRM | D Bi | Address Latch Enable input, multiplexed with SSP R2T frame output |
| 35 | CSn / R2T_CLK | D In | Active-low chip select active low, multiplexed with SSP R2T clock |



| Pin # | Pin Name | Type [†] | Description |
|----------|----------------------|-------------------|---|
| 36 | RDn / T2R_CLK | D Bi | Read strobe, active low, multiplexed with SSP T2R clock signal |
| 37 | WRn / R2T_D[0] | D In | Write strobe, active low, multiplexed with SSP R2T data signal |
| 38 | IRQn | D Bi | Interrupt, active low, Power-up state: HiZ |
| 39 40 | Dtest0 Dtest1 | D Bi | At the termination of reset, Dtest1 is sensed and is used to configure the digital pins for parallel or serial operation. Additionally, DTEST0 must be held low as the R1000 is coming out of reset to disable factory test mode behavior. |
| 41 | CLK_out | D Bi | Reference clock output for other chips |
| 42 | TCXO | Clk In | Reference clock input from a 24 MHz AC coupled TCXO |
| 43 | Vdd_clkref | 1.8 V | Supply of clock reference input buffer |
| 44 | Vdd_pll | 3.3 V | PLL Supply |
| 45 46 | PLL_fil0 PLL_fil1 | A | Nodes for external PLL filter |
| 47 | Vdd_vco | 3.3 V | VCO supply |
| 48 49 | Amp_Qp Amp_Qn | A In | Q post-mixer amplifier input |
| 50 51 | Mix_Qn Mix_Qp | A Out | Q Mixer output |
| 52 53 | Amp_Ip Amp_In | A In | I post-mixer amplifier input |
| 54 55 | Mix_In Mix_Ip | A Out | I Mixer output |
| 56 | Vdd_rx_ana | 3.3 V | RX analog supply |
| Paddle | GND | GND | Single Chip Ground |

[†]In the Type column, A denotes analog, while D denotes digital.

4 Electrical Specifications

4.1 Absolute Maximum Ratings

The absolute maximum ratings (see [Table 5](#)) define limitations for electrical and thermal stresses. These limits prevent permanent damage to the Indy R1000 reader chip.

Caution: Operation outside these maximum ratings might result in permanent damage to the device.

Table 5: Absolute Maximum Ratings

| Parameter | Min | Max | Unit | Conditions |
|------------------------------------|--------------|------------|-------------|--|
| Digital core supply voltage | -0.5 | 2.1 | V | Vdd_dig |
| Digital I/O supply voltage | -0.5 | 3.6 | V | Vdd_io |
| Analog PA supply voltage | -0.5 | 2.1 | V | Vdd_tx_pa/Vdd_tx_pre |
| Analog clock ref supply voltage | -0.5 | 2.1 | V | Vdd_clkref |
| Analog supply voltage | -0.5 | 3.6 | V | Vdd_pll, Vdd_rx_ana, Vdd_tx_ana, Vdd_tx_rf |
| Analog VCO supply voltage | -0.5 | 3.6 | V | Vdd_vco |
| Analog RF RX supply voltage | -0.5 | 5.5 | V | Vdd_rx_rf |
| Maximum voltage on non-supply pins | -0.5 -1.0 | 3.6 3.6 | V V | Outputs Inputs |
| RF input power | - | +15 8:1 | dBm VSWR | PA_out Rx, Detector, LO |
| Storage temperature | -45 | +85 | °C | |



4.2 Operating Conditions

This section shows operating voltage, frequency, and temperature specifications for the Indy R1000 reader chip. [Table 6](#) provides the supported operating conditions:

Table 6: Operating Conditions

| Parameter | Min | Typ | Max | Unit | Conditions |
|---------------------------------|-------|-----|-------|------|---|
| Digital core supply voltage | 1.7 | 1.8 | 1.9 | V | Vdd_dig |
| Digital I/O supply voltage | 3.135 | 3.3 | 3.465 | V | Vdd_io |
| Analog PA supply voltage | 1.7 | 1.8 | 1.9 | V | Vdd_tx_pa/Vdd_tx_pre |
| Analog clock ref supply voltage | 1.7 | 1.8 | 1.9 | V | Vdd_clkref |
| Analog supply voltage | 3.135 | 3.3 | 3.465 | V | Vdd_pll, Vdd_rx_ana, Vdd_tx_ana, Vdd_tx_rf |
| Analog VCO supply voltage | 3.135 | 3.3 | 3.465 | V | Vdd_vco |
| Analog RF RX supply voltage | 4.75 | 5.0 | 5.25 | V | Vdd_rx_rf |
| Analog supply ripple | - | - | TBD | mVp | For all supply rails Frequency of ripple TBD MHz |
| Digital supply ripple | - | - | TBD | mVp | Frequency of ripple TBD MHz |
| Operating temperature | -20 | - | +90 | °C | Case Temperature |

4.3 Transceiver Functional Specifications

Table 7a: Power Consumption Specifications in Mission Mode (Reading Tags) and Reset

| Parameter | Min | Typ | Max | Unit | Conditions |
|-------------------|-----|------|-----|------|------------|
| Power consumption | | 1250 | | mW | @ 17dBm |
| Power consumption | | 1000 | | mW | @ 12dBm |
| Power consumption | | 950 | | mW | @ 6.1dBm |

Power consumption measurements were taken from and based on the Indy R1000 Development Platform which should be representative of a real world application. Note: this data is based on a front end mixer power supply of 3.3V. Using a 5V rail for the front end mixer increases the P1dB of the mixer and increases power consumption by 200mW in high gain mode and 100 mW in low gain mode.

Table 7b: Indy R1000 Reader Chip - Receiver Specifications

| Power Rail Voltage | Typical after Reset Current (mA) | Tag Read Current (mA) | Voltage | Notes |
|--------------------|----------------------------------|-----------------------|---------|--------|
| P1.8V_RF | 6 | 205 | 1.8V | analog |
| P3.3V_RF | 195 | 226 | 3.3V | analog |
| P5V_RF | 17 | 17 | 5V | analog |

Table 8 shows nominal design values for R1000 power supply consumption.

Table 8: Indy R1000 Reader Chip - Receiver Specifications

| Parameter | Min | Typ | Max | Unit | Conditions |
|--|-----|-------------|-----|------------|--|
| Input frequency | 840 | | 960 | MHz | |
| Differential input impedance | | 50 | | Ω | Frequency = 900 MHz Note Recommended Balun in App Note |
| Differential input match | | 9 | | dB | S11 |
| Signal voltage gain | | 4 13 | | dB dB | Low gain path High gain path |
| Noise figure with jammer | | TBD TBD | | dB dB | LNA, mixer and LO Low gain path High gain path |
| Noise figure without jammer | | 11 14 | | dB dB | LBT high gain path LBT low gain path |
| Power level | | | | | |
| IIP2 | | +50 | | dBm | |
| I and Q phase error | | TBD | | deg | At IF output |
| I and Q amplitude error | | TBD | | dB | At IF output |
| LO leakage | | -60 | | dB | At RF input |
| IF bandwidth | | 10 | | MHz | |
| Chip sensitivity level (1% PER) | | -96.5 | | dBm | • FM0 40 kbps, IFLNA: High Gain, RF: High Gain, No Self-Jammer |
| | | -95 | | dBm | • Miller 4 62.5 kbps, IFLNA: High, RF: High, No Self-Jammer |
| | | -93.5 | | dBm | • FM0 40 kbps, IFLNA: High Gain, RF: Low Gain, No Self-Jammer |
| | | -92 | | dBm | • Miller 4 62.5 kbps, IFLNA: High Gain, RF: Low Gain, No Self-Jammer |
| In-channel RSSI dynamic range in low gain | TBD | -25 -85 | TBD | dBm dBm | Maximum level Minimum level |
| In-channel RSSI dynamic range in high gain | TBD | -45 -110 | TBD | dBm dBm | Maximum level Minimum level |
| RSSI register size | | 8 | | Bits | |
| Co-channel selectivity | | TBD | | | |
| Adjacent channel selectivity | | TBD | | | Dependent on external adjacent channel filter |
| Blocking and desensitization | | TBD | | TBD | Dependent on external adjacent channel filter |
| LO input power | -20 | | 0 | dBm | TBD |



| Parameter | Min | Typ | Max | Unit | Conditions |
|--------------------|-----|-----|-----|------|---------------------|
| LO input impedance | | 50 | | Ω | Frequency = 900 MHz |

Table 9: Indy R1000 Reader Chip - Transmitter Specifications

| Parameter | Min. | Typ. | Max. | Unit | Conditions |
|---------------------------------------|------|------------|------|------------|---|
| TX differential load impedance | | 50 | | Ω | Frequency = 900 MHz Output port of the Balun |
| TX output power | | +20 +10 | +17 | dBm dBm | Linear, P1dB Linear, Modulated |
| Linear mode OIP3 | | +27 | | dBm | |
| TX output power temperature variation | | | TBD | dB | CW with closed loop power control -20° to 75°C |
| TX output power absolute tolerance | | TBD | | dB | With closed loop power control |
| TX output power range | | 15 | | dB | Linear mode (Analog Resolution) |
| TX output power step size | | 2 | | dB | Linear mode (Analog Range) |
| AM control signal to external PA | | 0.7 | | Vp | |

Table 10: Indy R1000 Reader Chip External LO Input

| Parameter | Min | Typ | Max | Unit | Conditions |
|--------------------------|-----|-----|-----|------|------------|
| Input impedance | | 50 | | Ω | |
| Differential input match | | -9 | | dB | S11 |
| Input frequency | 840 | | 960 | MHz | |
| Input power level | -20 | | 0 | dBm | |
| Supply voltage | | 3.3 | | V | Vdd_tx_rf |

Table 11: Indy R1000 Reader Chip Envelope Detectors

| Parameter | Min | Typ | Max | Unit | Conditions |
|-----------------------------|------------|-----|------------|------------|----------------------------|
| Forward power detection | TBD | | TBD | dBm | At LO input |
| Reverse power detection | TBD | | TBD | dBm dBm | At detector input |
| Wideband listen before talk | TBD TBD | | TBD TBD | dBm dBm | At RX input At RX input |

Table 12: Indy R1000 Reader Chip Synthesizer

| Parameter | Min | Typ | Max | Unit | Conditions |
|---|-----|------|-----|--------|--|
| Frequency Range | 840 | | 960 | MHz | |
| Frequency Grid | | 25 | | kHz | Europe (ETSI 300 220) |
| | | 100 | | kHz | Europe (ETSI 302 208) |
| | | 250 | | kHz | US (FCC) |
| Reference Input Frequency | | 24 | | MHz | TCXO Specification |
| Reference Frequency Tolerance | | | 10 | ppm | TCXO Specification |
| Reference Input Level | | 0.8 | | Vp | |
| Reference Duty Cycle | 40 | | 60 | % | |
| PLL settling time within 1% of frequency step | | 140 | 470 | µs | 100 KHz grid, recommended PLL Loop filter configuration |
| TX Phase Noise | | -116 | | dBc/Hz | $\Delta f = 200$ kHz |
| Broadband Noise | | -144 | | dBc/Hz | $\Delta f = 3.6$ MHz |
| TX In-band spurious emissions | | -69 | | dBc | RBW = 3 kHz, average detector |
| TX Out-of-band spurious emissions measured with balun | | 54 | | dBm | Below 1 GHz (ETSI) RBW = 120 kHz, peak detector |
| | | -42 | | dBm | Above 960 MHz (FCC) RBW = 1 MHz, average detector |
| RX Spurious emissions | | -57 | | dBm | Measured with balun (and BPF) 30 MHz to 1 GHz 1 to 12.75 GHz |
| | | -47 | | dBm | |



Table 13: Indy R1000 Reader Chip Clock Output, DACs, and ADCs

| Parameter | Min | Typ | Max | Unit | Conditions |
|-------------------------------------|-----|----------------------------|-----|----------------------------|--|
| Maximum load capacitance on CLK_out | | 10 10 10 10 10 | | pF pF pF pF pF | Output clock rate 48 MHz 24 MHz 12 MHz 6 MHz 3 MHz |
| Antenna input detection range | 0.3 | | 2.7 | V | |
| Antenna input detection resolution | | 8 | | bits | |
| Temperature sensor range | 0.3 | | 2.7 | V | |
| Temperature sensor resolution | | 8 | | bits | |
| PA bias output range | 0.3 | | 2.7 | V | |
| PA bias resolution | | 8 | | bits | SD DAC implementation |
| PA regulator ctrl output range | 0.3 | | 2.7 | V | |
| PA regulator ctrl resolution | | 8 | | bits | SD DAC implementation |

Table 14: Indy R1000 Reader Chip Digital Interface

| Parameter | Min | Typ | Max | Units | Conditions |
|-----------------------|-----|-----|-----|-------|------------|
| Input high voltage | 1.5 | | Vdd | V | |
| Input low voltage | 0 | | 0.9 | V | |
| Output high voltage | 2.3 | | Vdd | V | |
| Output low voltage | 0 | | 0.7 | V | |
| Input leakage current | -10 | | 10 | μA | |
| Input pin capacitance | | | 10 | pF | |

5 Functional Description

The transmitter supports both in-phase quadrature (I-Q) vector modulation and polar modulation. The direct IQ up-conversion is intended for single sideband amplitude shift keying (SSB-ASK) and phase reversal amplitude shift keying (PR-ASK). The polar modulation is intended for double sideband amplitude shift keying (DSB-ASK). In both cases, the signals are generated in the digital domain and converted to analog signals by sigma-delta digital-to-analog converters followed by reconstruction filters. The integrated PA can be operated in three different modes:

- Class F with high output power and without internal amplitude modulation (AM)
The PA acts as a driver for an external PA. The AM is performed in the external PA, but it does require an external modulator.
- Class A required for SSB-ASK and PR-ASK
An optional linear external PA can be fitted to increase the output power to the maximum allowed level.

The baseband encoding and pulse-shaping is done with a lookup table to minimize latency. In the case of SSB-ASK transmission, the baseband signal is filtered with a Hilbert filter to create a complex IQ signal with suppressed negative frequencies. The signal is then offset in frequency to center the SSB-ASK spectrum in the channel. The digital I and Q signals are converted into the analog domain by sigma-delta DACs.

In DSB-ASK transmission, the baseband encoding and pulse shaping is performed in the same manner as it was for SSB-ASK, but the shaped signal is pre-distorted to compensate for non-linearity in the AM transfer function. The pre-distorted AM control signal is converted into the analog domain by the I and Q sigma-delta DACs as defined in the lookup tables.

The receiver is in principle a homodyne to ensure that as much as possible of the transmitter (TX) leakage falls on DC. The receiver downconversion mixer can be driven either by the internal local oscillator (LO) signal or by an external LO signal typically tapped off from the output of the external PA. The receiver uses a single on chip low noise amplifier (LNA). If the system needs to accommodate a +10-dBm jammer, a 4-dB external attenuator is required.

After downconversion, the major part of the DC is removed by resettable AC-coupling capacitors. The analog intermediate frequency (IF) filter provides coarse channel selectivity. It has programmable bandwidth to accommodate for the large range of required data rates. The coarsely filtered I and Q signals are analog-to-digital converted. Automatic IF gain stepping in the filter reduces the required dynamic range of the ADC. Sharp and well controlled digital filtering supplements the coarse analog filtering. The demodulation is also performed digitally.

The clocks for the digital blocks are derived from a 24-MHz reference frequency originating from an external temperature compensated crystal oscillator (TCXO). The sigma-delta DACs run directly on the 24-MHz signal. The sigma-delta ADCs run on a 48-MHz clock generated by an integrated frequency doubler.

The VCO is fully integrated. The loop filter is external for the synthesizer to meet the stringent phase noise requirements. The time reference required by the phase locked loop (PLL) and the digital blocks is derived from the 24-MHz reference frequency.

The Indy R1000 reader chip supports two interfaces, one low speed parallel interface with a data rate of up to 20 Mbps, and one serial interface with a data rate of 150 Mbps to the Indy R1000 reader chip and up to 450 Mbps from the Indy R1000 reader chip. The interfaces are multiplexed on the same pins, and the interface is determined during power-up. Both interfaces are operated at 3.3 V. Low level instructions are written into a first in, first out (FIFO) buffer and executed one at a time by the Indy R1000 reader chip. All information is transferred via the register bank. The control of the Indy R1000 reader chip is state machine driven.

5.1.2 LO Input

The RX LO may be sourced internally or externally as shown in [Figure 6](#). If an external RX LO is not used, the DC blocking capacitors, inductor, and balun are not required.

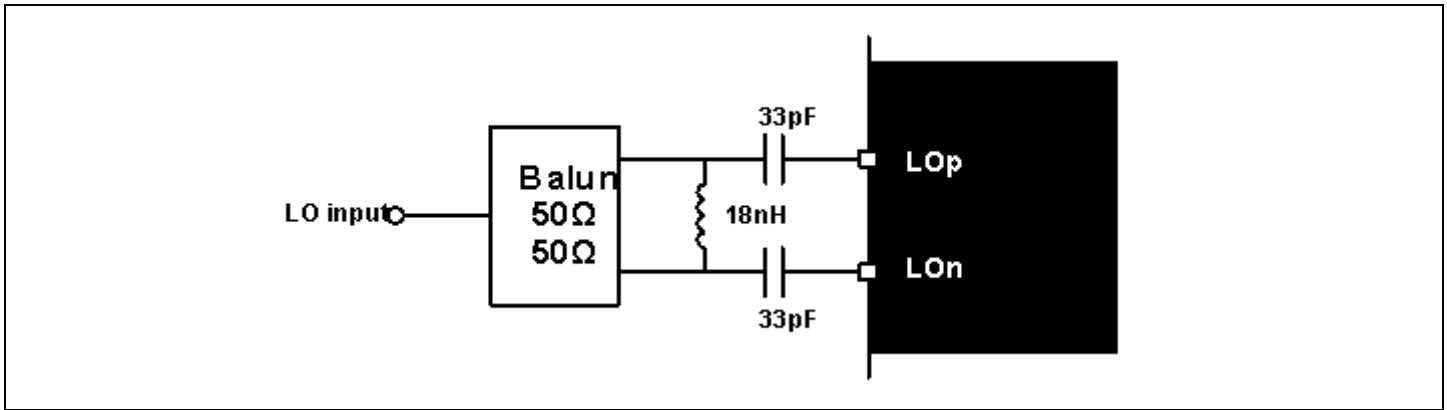


Figure 6: LO Input External Interfaces

5.1.3 Receive RF Interface

The Indy R1000 reader chip has differential RF and LO ports to alleviate interference on the package bond-wires coming from the digital section of the chip.

The Indy R1000 RX Mixer also supports a high gain and a low gain mode with differing compression points. In order to switch between these modes, it is necessary to both correctly program the ANA_CTRL1 register as well as bias the output of the mixer to +3.3v through 400 ohm resistors. These resistors may be switched in for low gain mode and out for high gain mode. Ensure that when switched out, these bias resistors do not create an unintended current summing node.

5.1.4 Receive Baseband Interface

An AC coupling interface is used in the Indy R1000 reader chip between the mixer and the baseband low noise amplifier. This interface provides a high-pass filtering response to notch out the DC offset generated by the self-jamming signal from the transmitter.

The design of the baseband interface meets the following requirements:

- The high-pass filtering corner must be low enough to not attenuate the received signal. Although the tag response modulation does not consist of any DC content, the low data rate modes can have significant signal contents very close to DC
- The high-pass filtering corner must be high enough so that the DC changes can converge quickly enough. There is a change of DC content going from modulated data transmission (interrogator transmit) to continuous wave (CW) transmission (interrogator receive.) The DC changes need to converge before the receive demodulator can demodulate correctly. The DC level change occurs during transition from transmit to receive. Varying the time constant of the high-pass filtering or sampling and holding the DC offset is allowed, provided the air interface protocol is not violated.
- The AC coupling capacitor and the bias resistance must form a low-pass filter for the bias thermal noise, provided the total integrated noise is a constant equal to KT/C . To reduce the input referred noise of the baseband low noise amplifier, either make the corner frequency high to lower the in-channel spectral noise density, or make the corner frequency lower than the high-pass filtering in the baseband filter chain.

To increase the noise bandwidth corner, ensure the following requirements are met:

- The input impedance into the baseband amplifier must be high.
- The coupling capacitor can be small; however, the high-pass DC notch corner may be too high.

To lower the noise bandwidth, ensure the following requirements are met:

- The input impedance into the baseband amplifier can be low.
- The coupling capacitor must be large. The requirements are as follows:
 -
 - The AC coupling capacitor must be charged within the protocol allowed wake-up time.¹
 - The high-pass filter in the baseband filter chain must attenuate the noise under the receiver noise floor.
 - The choice of AC coupling capacitor size must be made in conjunction with the low noise baseband amplifier design.

5.2 Digital Receiver Data Path

The receive path sigma-delta ADC is followed by a fixed decimation chain with a decimation factor of 16. To keep the relationship between signal bandwidth and the filter sample rate relatively constant for efficient use of the main digital filter, an additional data rate dependent decimation is employed.

The digital channel filtering is a combination of a 36- or 72-tap finite impulse response (FIR) filter configurable in steps of six taps and a second order infinite impulse response (IIR) filter. Both filters have programmable coefficients with some limitations (Register 0x221). The FIR filter is typically programmed to be a fast roll-off low-pass filter. The IIR filter is typically a low-pass Butterworth filter with very low cutoff frequency to estimate the DC, which is then subtracted from the FIR filter output. Another possible configuration is to disable the IIR filter, causing its output to be forced to zero, and instead implementing a bandpass filter directly with the FIR filter. It is possible to completely bypass the digital filtering if desired as well. The signals both before and after the digital filter can be accessed and forced to manually set values through override registers.

The digital channel filter block is followed by the phase recovery block. This block aligns the modulation with the real-axis, i.e., all the information is in the I-signal. This block also derives the instantaneous narrowband received signal strength indicator (RSSI). A separate RSSI block averages these instantaneous values over a programmable number of samples and calculates the log 2 of the received signal amplitude.

5.2.1 Decimation Filters and AGC Control

The single-bit sigma-delta ADC is followed by four polyphase decimation filters with fixed coefficients. The coefficients of the first and second decimation filters are identical. The first decimation stage is decimate by 16. The second and third filters have 9 and 15 taps, respectively. Amplitude information used to control the gain settings in the analog AGC is tapped off after the third decimation filter to ensure the measurement bandwidth is at least as large as the analog filter bandwidth. The additional data rate dependent decimation is based on a series of identical 13-tap polyphase decimation filters. Rate dependent decimation is programmable to 1, 2, 4, or 8.

¹ Possibly, the charging time for the AC coupling capacitor can be improved with the help of a low resistance switch to short the capacitor during the charging up phase. This approach will lower the time constant to enable a fast charge phase even with a big value AC coupling capacitor.

5.2.2 Digital Channel Filter

The AC coupling after the mixer removes the major part of the DC; however, the DC content coming into the digital filter is for weak tag responses and still much larger than the amplitude modulation of the signal. To ensure robust preamble detection, the DC has to be reduced at the very beginning of the packet. The DC is estimated by a second order Butterworth IIR filter and subtracted from the output of the FIR filter. The group delay of the FIR filter is approximately the same as the low frequency group delay of the IIR DC estimation filter. This means that good DC suppression is possible at the very beginning of the preamble. During the last few bits of the packet, the output of the DC estimation filter must be held for optimum performance.

Both the FIR and IIR filters are programmable with some limited restrictions. The FIR filter must be symmetric. It is not possible to shorten the group delay by setting the filter pre-cursor to zero, but it is possible to shorten the group delay by reducing the length of the filter. The signal input is injected into the first utilized filter tap. Therefore if the filter length is reduced, the data bypasses some data delay elements. The IIR filter coefficients must be normalized so that a_0 , b_0 , and b_2 are all equal to one. Both the FIR and IIR coefficients must be real; i.e., it is not possible to distinguish between positive and negative frequencies in these filters.

5.2.3 RSSI

Received signal strength information is derived from amplitude information available in the phase recovery block. The information made available in the RSSI register is proportional to \log_2 of the received signal amplitude. The information is averaged over a programmable number of samples as defined in register 0x281. The start time is defined in 0x280. The minimum specified level will be below the integrated noise floor for many IF filter bandwidth settings.

5.3 Digital Transmitter Data Path

The input to the TX data path is baseband encoded and shaped data from the controller for both the I and Q branches of the data path. For SSB, only the I output is used and the Q values are created by the Hilbert transformer. A frequency offset is added using a COordinate Rotation Digital Computer (CORDIC) block to center the spectrum in the channel.

In DSB operation, the DSB signal can be pre-distorted before being fed either through an upsampling or directly to the DAC. To allow for high bandwidth signals in C1G1, there is a bypass possibility at the DAC. This makes it possible to toggle the output of the DAC using a single bit.

The output `txpsk_phase`, which is the sign bit of the DAC input, is provided for testing PR-ASK using polar modulation. The signal has a programmable delay to compensate for the delay in the reconstruction filter and other analog parts.

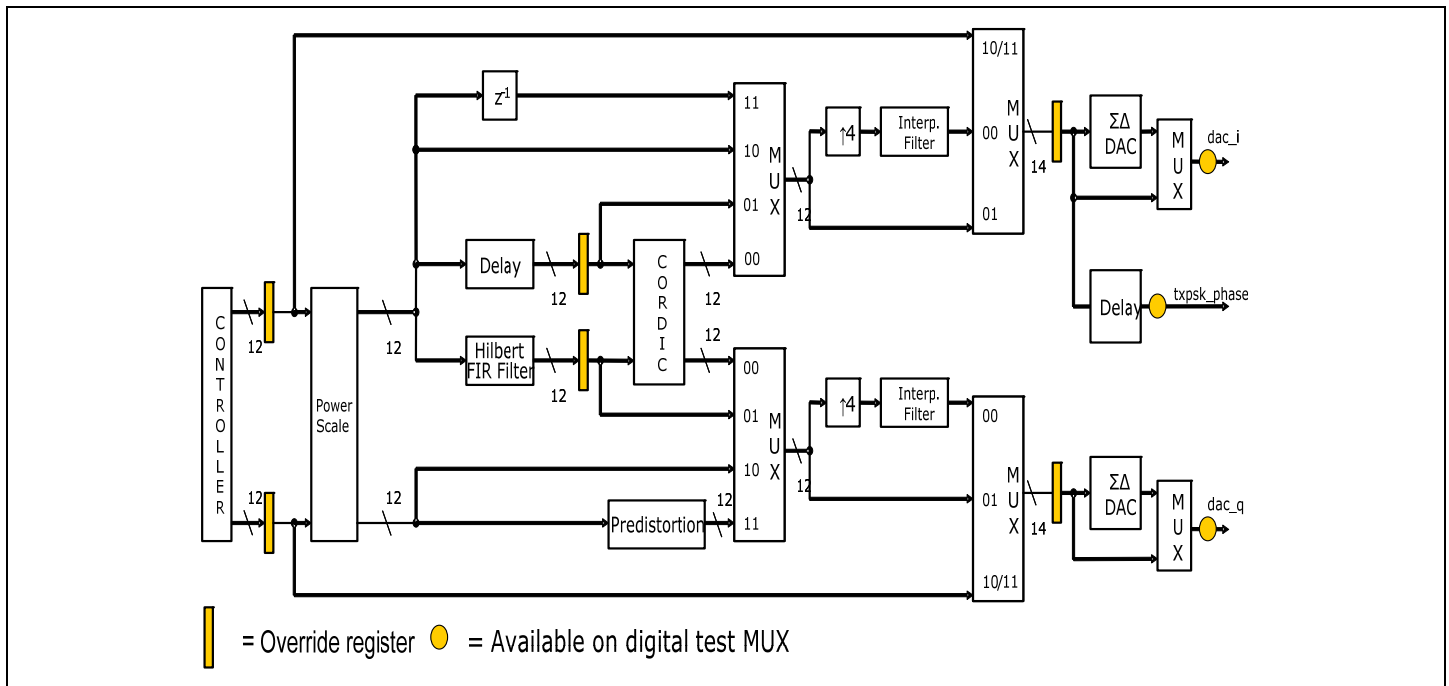


Figure 7: Overview of the Digital Part of the Transmitter Data Path

5.3.1 Baseband Encoding and Pulse Shaping

The baseband encoding and pulse shaping is performed simultaneously using a fully programmable lookup table. The lookup table is part of the register map, and the encoding is done in the controller. For each of the branches, I and Q, 64 samples are stored. The 64 samples are fully addressable, but the addresses to the I and the Q tables are linked. The controller can output up to 32 samples per access.

Table 15: Specification of Baseband Encoding and Pulse Shaping Block

| Parameter | Min | Typ | Max | Unit | Conditions |
|--------------------------------|----------------|-----|------|-------|------------|
| Output sample rate | | | 4.0 | Msp/s | |
| Programmable registers | 2 x 64 samples | | | | |
| Register and output data width | | 12 | | bits | |
| Register and output range | -2 | | 1.99 | | |

5.3.2 Power Scaling

The power scaling block is a multiplier in which the input is multiplied with a programmable value. The gain of the I and the Q channels can be programmed independently.

5.3.3 Hilbert Transformer

The Hilbert transformer is used to generate a SSB signal from a DSB AM signal. The coefficients are anti-symmetric, and every second coefficient is zero (the first being non-zero). All non-zero coefficients are programmable. The order of the filter can be programmed to two discrete values: 22 and 10. When the 10th order Hilbert transformer is used, all coefficients that are not used must be programmed to zero. The 10th order Hilbert filter is used to avoid ISI in the modulated data.

5.3.4 Frequency Shifter

The frequency shifter is used for shifting the spectrum in SSB mode so that it is centered in the middle of the channel. It is also used for shifting the LO in listen before talk (LBT). The frequency shifter is based on the CORDIC algorithm.

5.3.5 AM Pre-distortion

AM pre-distortion uses a fifth order polynomial work function. This equation defines the function, where x is the input and y is the output of the block.

$$Y = C_0 + C_1 \cdot X + C_2 \cdot X^2 + C_3 \cdot X^3 + C_4 \cdot X^4 + C_5 \cdot X^5$$

The coefficients C_0 through C_5 are programmable. This function is used during DSK-ASK polar modulation.

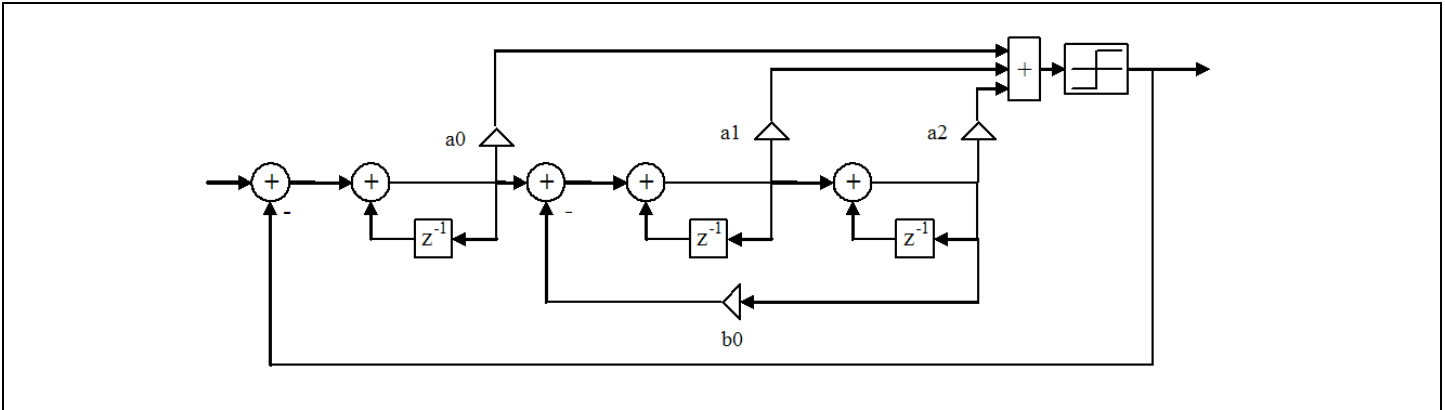
5.3.6 Upsampling

For low data rates, the baseband signal needs to be upsampled and filtered prior to the oversampling of the DAC. This process suppresses the images at multiples of the original sample rate. For modes with a high sample rate or when spectral purity is of lesser concern, the upsampling can be bypassed.

The upsampling uses a standard upsample and filter approach. The filter is a 17th order FIR filter with fixed coefficients.

5.3.7 Sigma Delta Digital to Analog Converter

The conversion from digital to analog is performed by a third order sigma-delta DAC. The structure of this DAC is illustrated in [Figure 8](#), and the specification values are provided in Table 16.


Figure 8: Principle of Sigma-delta DAC
Table 16: Specification of Sigma-delta DAC

| Parameter | Min | Typ | Max | Unit | Conditions |
|----------------------------|------|---------------|-----|-------|--------------------------------|
| Order | | 3 | | | |
| Input sample rate | | | 6.4 | Msp/s | |
| Output sample rate | | 24 | | Msp/s | |
| Input data width | | 14 | | bits | |
| Input data scaling | | 0.5 | | | |
| Output data width | | 1 | | bit | |
| Input amplitude | -0.5 | | 0.5 | | (Stable region) |
| Signal to noise ratio | TBD | 74 | | dB | Integrated noise in 300 kHz BW |
| Feed-forward coefficient 0 | | 0.5 | | a0 | |
| Feed-forward coefficient 1 | | 0.1875 | | a1 | |
| Feed-forward coefficient 2 | | 0.033203125 | | a2 | |
| Resonator coefficient | | 0.00341796875 | | b0 | |

5.4 Antenna Configuration Scenarios

There are two different use scenarios for the Indy R1000 reader chip based on the antenna subsystem. The first one involves a single antenna configuration as shown in [Figure 9](#). In this application, a circulator is used to isolate the transmit and receive paths. Although the figure illustrates the more general case where two (or more) physically separated antennas are controlled by a switch, each antenna performs the RX and TX function. The antenna reflection of CW transmit power in receive mode dominates the receiver compression point requirement. With a maximum transmit power at the antenna port of +30 dBm and assuming an antenna reflection loss of 15 dB, an in-band blocker of +15 dBm must be tolerated at the receiver input. In this configuration, an external pad is connected at the Rx_in port to avoid compression of the LNA. A high impedance tap at the output of the PA is implemented to generate the LO_in signal used to drive the RX mixers.

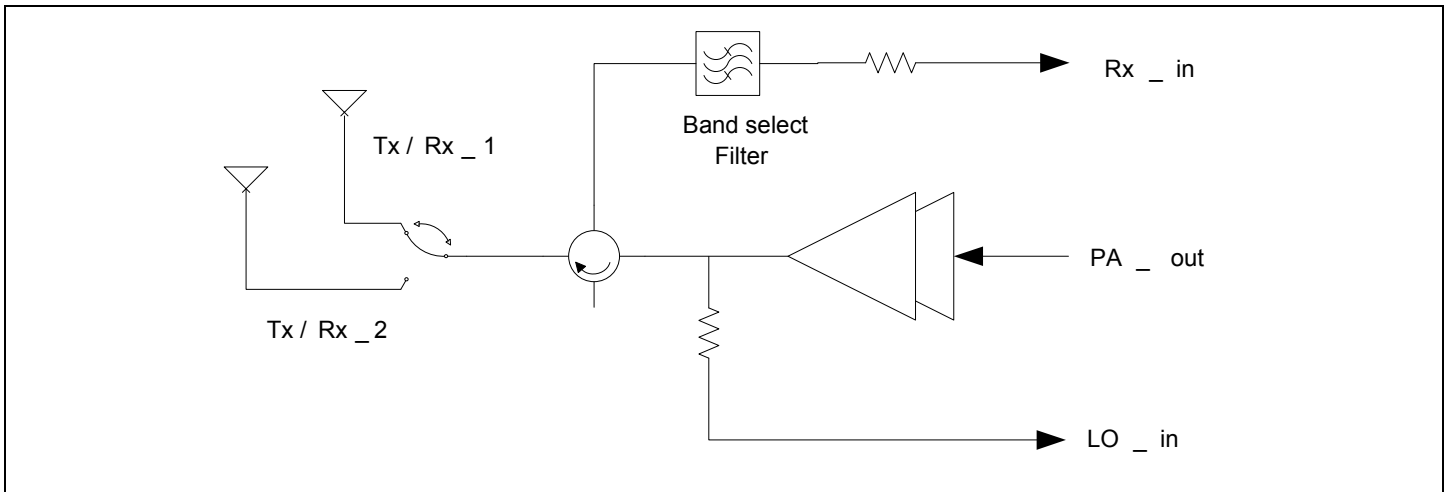


Figure 9: Single Antenna Scenario

A second scenario allows separate antenna connections for receive and transmit as shown in [Figure 10](#). The figure illustrates the more general case where two (or more) physically separated antennas are controlled by a switch, with each antenna only performing the RX or TX function. The isolation between the receive and transmit antennas is 25–30 dB; therefore, the in-band blocker caused by the CW transmit signal is in the order of +0 dBm. This scenario significantly reduces the compression requirements on the receiver and allows for a more sensitive receiver. A high impedance tap at the output of the PA is implemented to generate the LO_in signal used to drive the RX mixers.

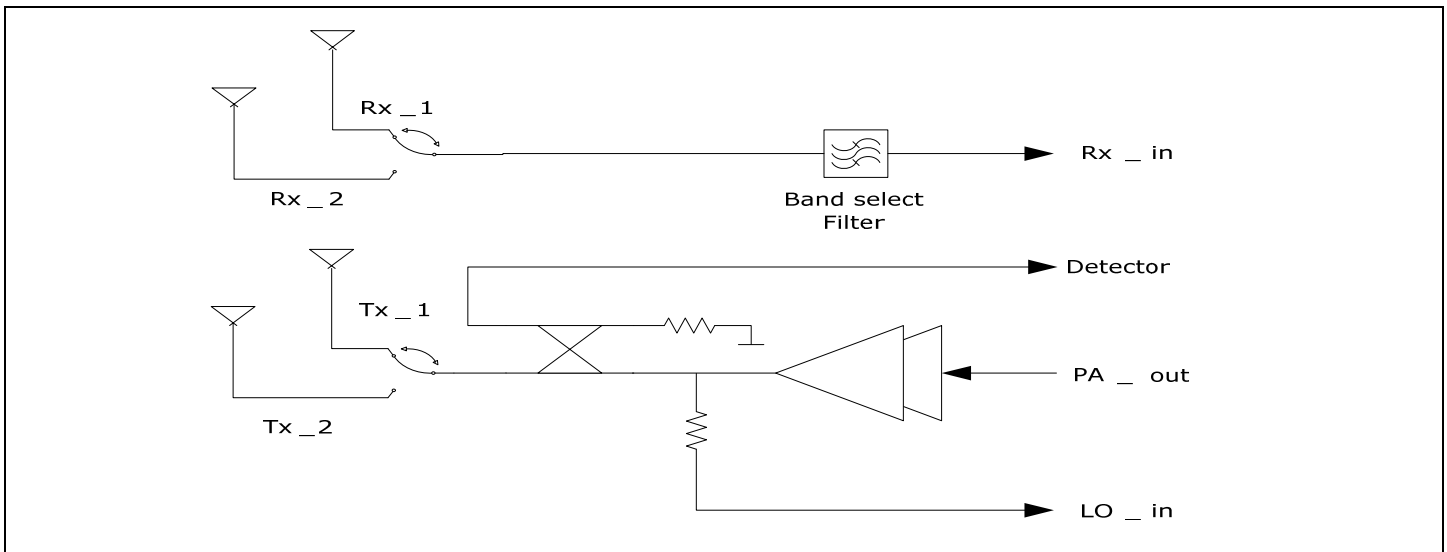


Figure 10: Dual Antenna Scenario

5.5 RF Power Detection

There are three power detection functions provided in the Indy R1000 reader chip:

- Forward power detection for transmit power calibration
The power is tapped after the PA using the same high impedance node used to generate the RX LO signal. This power detection is part of the transmit power calibration as well as part of the PA_regulator loop that controls the voltage supply for the PA.
- Reverse power detection for measuring antenna reflection
If a severe mismatch is detected, the controller shuts down the transmit PA to avoid it being damaged.
- Rough wideband LBT
High power (~ -30 dBm) activity is detected in the complete receive band, as defined by the external band select filter, and in the IF band following the down-conversion mixers.

There are power detectors at the input of the LO_in, Rx_in, and Detector signals in the Indy R1000 reader chip. In the single antenna configuration (see [Figure 9](#)), the power detector at the LO_in signal performs the forward power detection function and the power detector at the Rx_in signal is for the reverse power detection. The power detector at the Rx_in signal can also be used to implement a rough wideband LBT function with the transmitter turned off. A small RF amplifier may be switched on to slightly improve the sensitivity of the LBT detector. The peak detectors at the output of the IF amplifiers are connected to the auxiliary (AUX) ADC and can also be used to perform rough LBT.

In dual antenna configuration (see [Figure 10](#)), the power detector at the LO_in signal performs the forward power detection function. The power detector at the detector signal is used to measure the reverse power detection via a directional coupler. The power detector at the Rx_in signal can be used to implement a rough wideband LBT function with the transmitter turned off. A small RF amplifier may be switched on to slightly improve the sensitivity of the LBT detector.

5.6 Transmitter Modes

The Indy R1000 reader chip can operate in one of three transmitter modes, based on the power requirements and the modulation scheme used. These modes are described in this section.

5.6.1 Full Power Non-linear Mode (DSB-ASK)

An external PA is needed to transmit the maximum allowable power of up to +30 dBm at the antenna. To improve the power efficiency of the system, a Class-C polar modulation approach is used. The PA_out signal in the Indy R1000 reader chip drives in CW mode the gate of the PA transistor into Class-C operation. The drain of the PA transistor is amplitude modulated via a PA_modulation DAC. Discrete devices are used to interface between the two different voltage domains (see [Figure 11](#)). DSB-ASK is the only modulation supported in this mode.

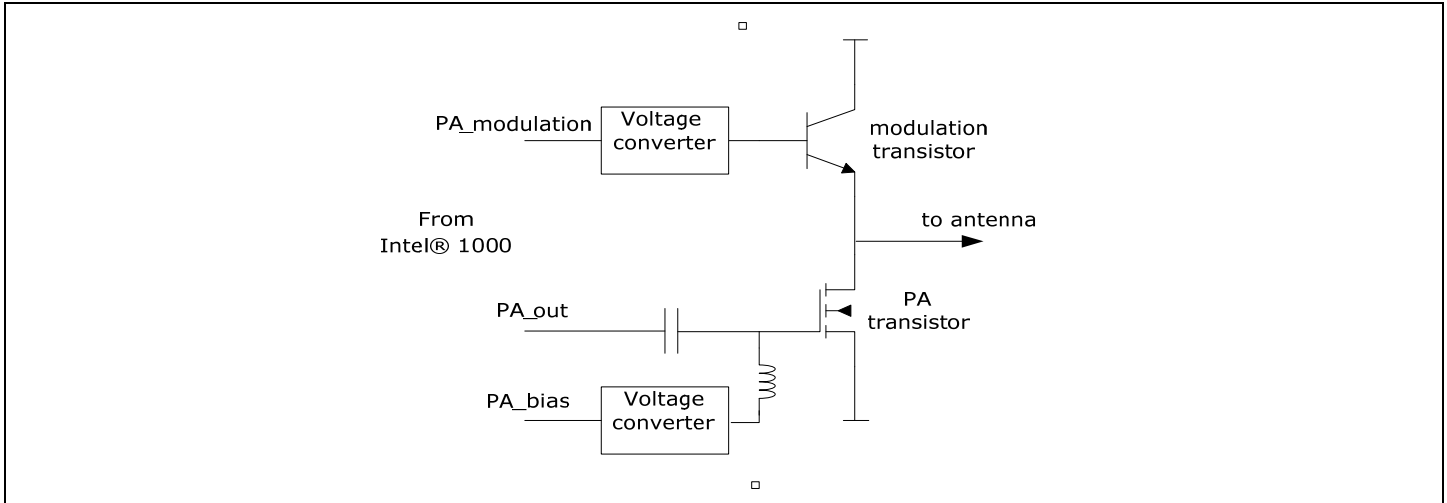


Figure 11: Indy R1000 Reader Chip Transmit with External PA (DSB ASK or PR-ASK)

5.6.2 Low Power Non-linear Mode (DSB-ASK)

The power control for this mode is similar to the full power mode, except that no external PA is used. Instead, an on-chip PA with lower output power is used. DSB-ASK is the only mode available in this configuration.

5.6.3 Linear Mode

In this mode, the PA_out signal in the Indy R1000 Reader Chip interfaces with an external linear PA, because SSB modulation requires a linear PA. The device is also able to generate DSB- and PR-ASK using the IQ upconverters and the linear on-chip amplifier.

6 Device Control and Programming

The Indy R1000 reader chip provides a high speed synchronous serial interface for programming the control settings and RFID protocol.

The interface to the microcontroller supports two different communication types:

- Low speed parallel interface (20 Mbps)
- High speed serial interface (150 Mbps downstream and 450 Mbps upstream)

Both interfaces use the same pins and are configured through the strapping options shown in [Table 17](#). Note: the parallel interface is not supported for new designs. The high speed serial interface is recommended for all applications.

Table 17: Strapping Options

| Mode | Pin Setting | | Description |
|------------------------------------|---------------|---------------------------------|--|
| Normal mode, Parallel interface | SCAN_test = 0 | Chip_resetrn = 1 Dtest1 = 1 | Indy R1000 reader chip is in normal operation mode using the parallel interface. |
| Normal mode, Serial interface | SCAN_test = 0 | Chip_resetrn = 1, Dtest1 = 0 | Indy R1000 reader chip is in normal operation mode using the serial interface |
| Factory Test Mode | SCAN_test = 1 | X | All analog blocks are disabled and the chip is put into factory test mode. |

Table 18: Pin Functionality Per Modev

| Pin Name | Parallel Interface | Serial Interface |
|--------------|--------------------|------------------|
| chip_resetrn | | |
| SCAN_test | Scan mode | Scan mode |
| CLK_out | | |
| Dtest0 | Dtest0 | Dtest0 |
| Dtest1 | Dtest1 | Dtest1 |
| IRQn | IRQn | IRQn |
| CSn | CSn | r2t_clk |
| ALE | ALE | r2t_frm |
| RDn | RDn | t2r_clk |
| WRn | WRn | r2t_dat |
| DA3 | DA3 | t2r_frm |
| DA2 | DA2 | t2r_dat[2] |
| DA1 | DA1 | t2r_dat[1] |
| DA0 | DA0 | t2r_dat[0] |

6.1 Serial Interface

The serial interface has four channels: one going to the Indy R1000 reader chip (R2T) and three coming from the Indy R1000 reader chip (T2R). Each direction has its own clock and frame synch signals (R2T_CLK, T2R_CLK and T2R_FRM, R2T_FRM). The channels are denoted as T2R_D0 and R2T_D0-2.

The data is transferred in 32-bit frames delimited with the frame synchronization signal. The data is sent most significant bit (MSB) first, and the frame synchronization must occur one bit period before the MSB of the frame. When data is transferred from the Indy R1000 reader chip (read request), it is placed on the lowest channel available. Up to 16 read responses can be queued in the Indy R1000 reader chip. The format of the data frame is shown in [Figure 12](#).

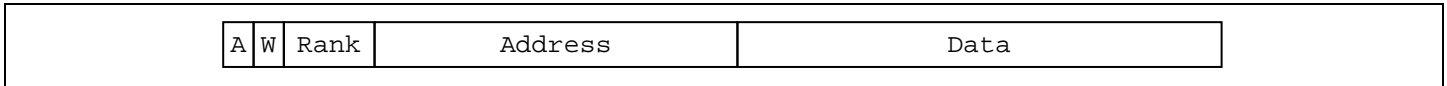


Figure 12: Serial Interface Frame Format

The A parameter determines if this access is valid or if it is an empty frame. The W parameter is set if the frame is a write operation. For T2R, this value is always zero. If the same source is read several times, the rank parameter determines the order of the incoming frames. For R2T transfers, this value is always zero. To perform a read request, the data field must be set to zero.

With the serial interface, there is an additional possibility of auto-reading certain registers. When this feature is enabled each time, the source register is clocked and the value is placed as a read request in the T2R FIFO. The timing parameters for the serial interface are shown in [Figure 13](#) and [Figure 13](#): Serial Interface T2R Timing

, and the timing requirements for the serial interface are specified in [Figure 14](#): Serial Interface R2T Timing

Table 19.

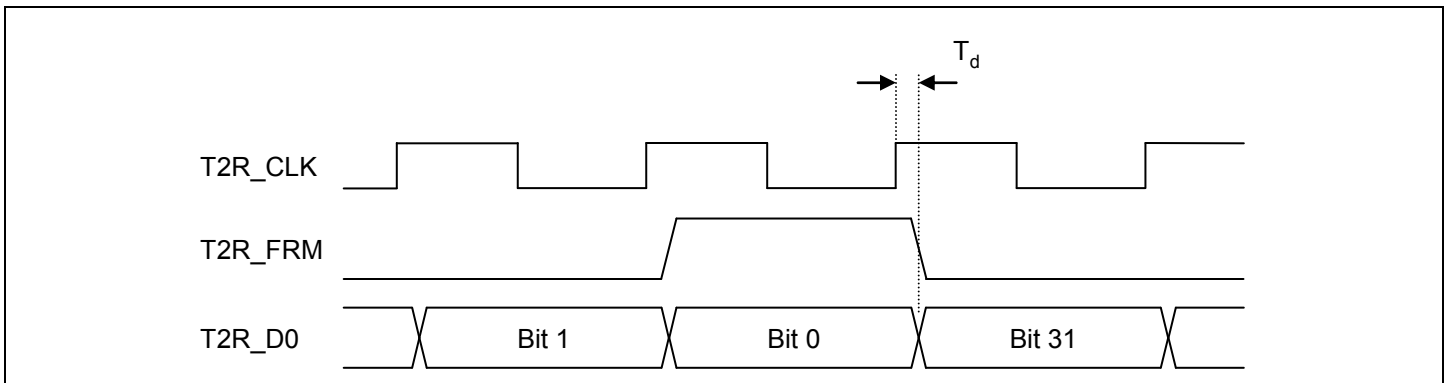
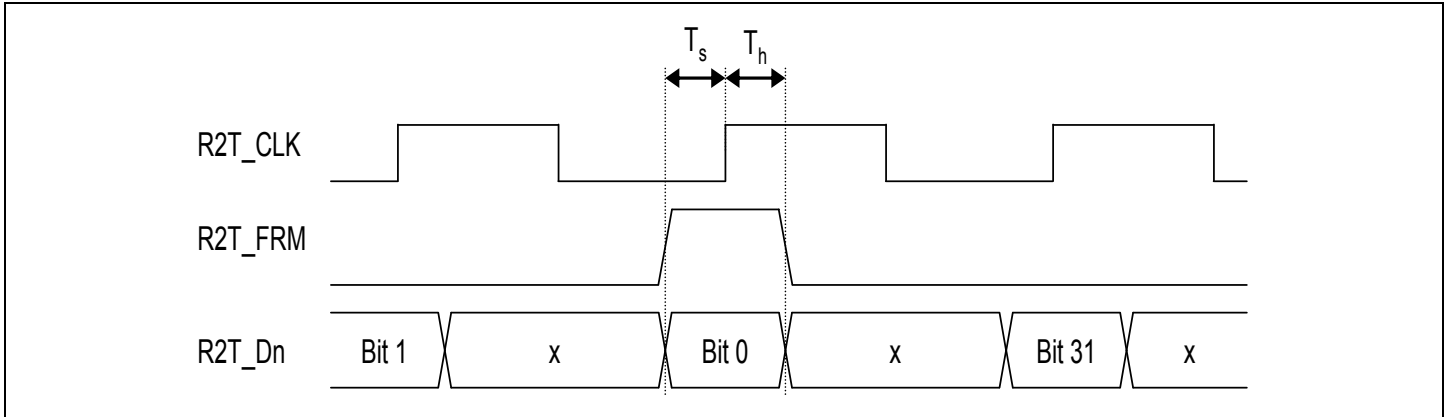


Figure 13: Serial Interface T2R Timing


Figure 14: Serial Interface R2T Timing
Table 19: Serial Interface Timing Requirements

| Symbol | Parameter | Min [ns] | Typ [ns] | Max [ns] |
|--------|-------------------|----------|----------|----------|
| T_d | Data output delay | 2.0 | | 5.0 |
| T_s | Data setup time | | 1.0 | |
| T_h | Data hold time | | 2.0 | |

6.1.1 Parallel Interface

The parallel interface is 4-bit wide with multiplexing of the data and address. The registers are double buffered to avoid mid-read updates. The read timing of the parallel interface is shown in [Figure 15](#), while the write timing is shown in [Figure 16](#): Parallel Interface Read Timing

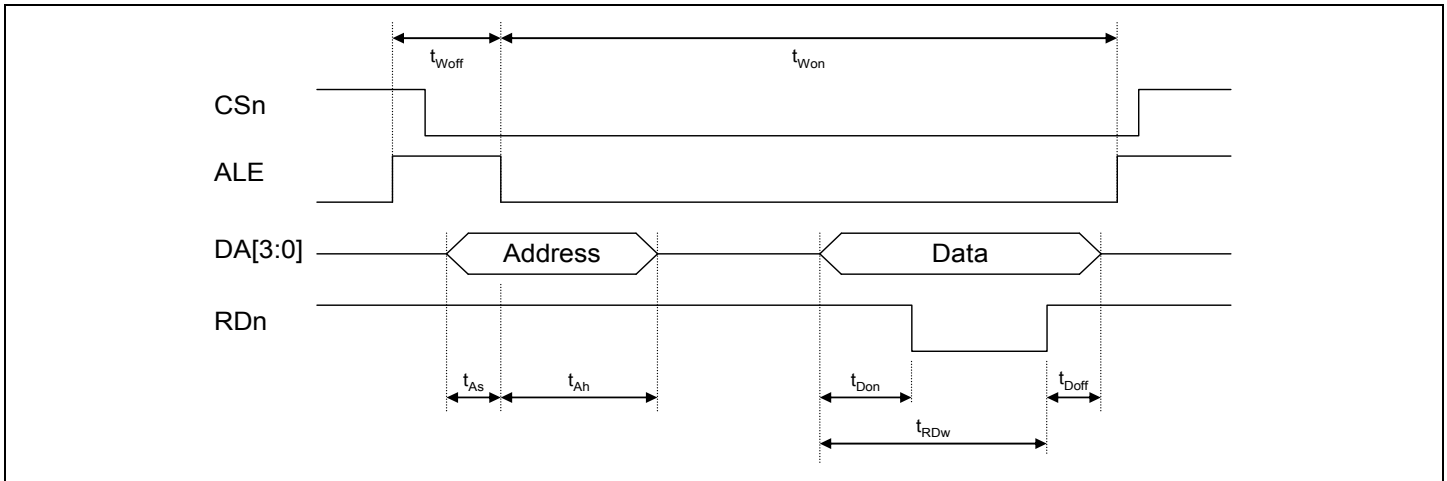


Figure 15: Parallel Interface Read Timing

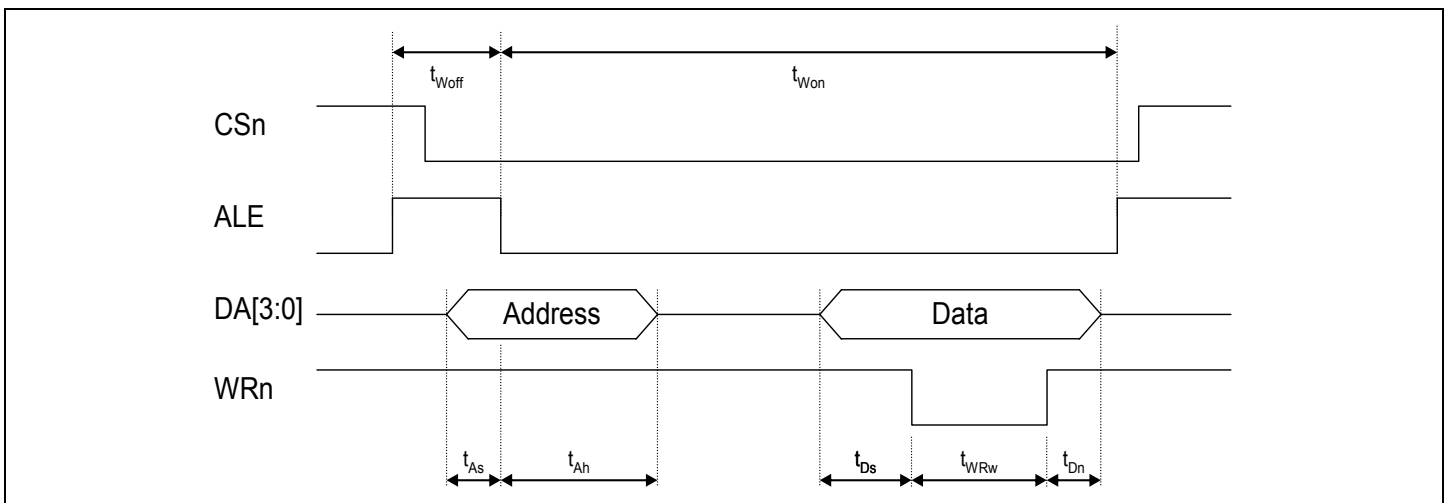


Figure 16: Parallel Interface Write Timing

**Table 20: Parallel Interface Timing Conditions**

| Symbol | Parameter | Min [ns] | Typ [ns] | Max [ns] |
|-------------------|-------------------------|----------|----------|----------|
| $t_{W_{on}}$ | ALE pulse width | 100 | | |
| $t_{W_{off}}$ | ALE inactive width | 100 | | |
| t_{As} | Address setup time | 4 | | |
| t_{Ah} | Address hold time | 0 | | |
| t_{RDW}/t_{WRW} | Read/Write strobe width | 50 | | |
| t_{Don} | Data-on output delay | 0 | | 45 |
| t_{Doff} | Data-off output delay | 0 | | 45 |
| t_{Ds} | Data setup time | 4 | | |
| t_{Dh} | Data hold time | 0 | | |

6.2 Register Map

Table 21: Direct Register Map, B Revision

| Addr. | Name | R/W | Bit | Description | Reset | Comment |
|-------|---------------------|-----|------------------------------------|---|-------|--|
| 3:0 | T2R ISO 18000-6C | R | 15:12 11 10:8 7:0 | Not Used Data valid Number of valid bits Received data | h0000 | Receive FIFO 16 Words deep In the number of valid bits 0 means full byte, 1 means 1 bit, etc. |
| | R2T Data Command | W | 15:12 11:8 7:4 3:0 | Argument (arg2) Argument (arg1) Argument (arg0) Command selection (cmd) | h0000 | Transmit FIFO, 16 Words Deep The command selection sets the data command to be performed: cmd = b0000: Data-0 cmd = b0010: Data-1 cmd = b0100: Reserved. cmd = b0110: Bin-pulse, arg0 specifies the bin number (0–7). Bin-Pulse 8 is the tag set-up window. cmd = b1000: Null cmd = b1100: Byte stored in arg1 and arg0. cmd = b1110: Send random sequence. Specified in 32-bit packets in arg2-arg0, zero = 4096 packets and one = 1 packet. The command selection shall be set to b01. For lines to execute and lines to loop a zero value means execute/loop one line. The start line is the offset in the microcode, starting in register h080. |
| | Non-data command | W | 15:11 10:9 8:6 5:2 1:0 | Number of loops Lines to loop Lines to execute Start line Command selection | | |
| | End of transfer cmd | W | 15:4 3 2:0 | RX delay Enable digital RX Command selection | | The command selection shall be set to b011. RX delay is the delay (in 24 MHz clock cycles) to wait after the EOT command is read from the FIFO before enabling the digital part of the receiver. |
| | Measurement cmd | W | 15:10 9 8 7:4 3 2:0 | RSSI delay Enable digital RX Enable RSSI AUX ADC select Not used Command selection | | The command selection shall be set to b111. The AUX ADC select is the channel for the ADC to measure. Turning on the RSSI and the digital part of the receiver is optional. The RSSI measurement can be offset from the receiver start by specifying the RSSI delay. |

| | | | | | | |
|-----|---------|-----|--|---|-------|--|
| 5:4 | DP_STAT | R | 7:4 3:0 | RX FIFO status TX FIFO status | h0000 | <p>Both the RX and the TX FIFO has 16 positions.</p> <p>The RX FIFO status is the number of free positions in the FIFO. Zero value of the status means both full FIFO and one position empty.</p> <p>The TX FIFO status is the number of occupied positions in the FIFO. The value hF means both full FIFO and one position empty.</p> |
| | DP_CTRL | W | 7 6:4 3 2:0 | Flush RX FIFO RX FIFO watermark Flush TX FIFO TX FIFO watermark | h0044 | <p>The RX watermark is for overflow while the TX watermark is for underflow. The watermark is indicated through an interrupt. For the RX FIFO the interrupt is only asserted on writes to the FIFO and for the TX FIFO the interrupt is only asserted of reads.</p> <p>The watermarks are set to 4 by default.</p> <p>Writing the flush bit only clears the FIFO once.</p> |
| 8:6 | IAR | R/W | 11:0 | Indirect address | h0000 | |
| c:9 | IDR | R | 15:0 | Read indirect data | h0000 | Reading address 9 performs the read; i.e., the read ends with address 9. |
| | IDR | W | 15:0 | Write indirect data | h0000 | Writing address 9 performs the write; i.e., the write ends with address 9. |
| f:d | ISR | R | 11 10 9 8 7 6 5 4 3 2 1 0 | Lock detect change IF LNA too low IF LNA too high Non-empty RX FIFO AUX ADC done SDI RX FIFO overflow RX FIFO at watermark RX time-out RSSI done ADC input overdriven Read from TX FIFO TX FIFO at watermark | h0000 | <p>Interrupt register:</p> <p>The interrupts are cleared nibble by nibble on read.</p> <p>The TX and RX watermark interrupts occurs <i>only</i> when the number of entries in the FIFO is exactly at the offset specified by the watermark.</p> |

Table 22: Indirect Register Map, B0 Stepping

| Addr. | Name | R/W | Bit | Description | Reset | Type | Comment |
|---------|------|-----|------|---------------------|-------|-------|--|
| 000-03F | TX_I | R/W | 11:0 | TX amplitude data I | h0000 | s1.10 | TX look-up table (LUT) amplitude data for the I-output (signed), 64 registers. |
| 040-07F | TX_Q | R/W | 11:0 | TX amplitude data Q | h0000 | s1.10 | TX look-up table (LUT) amplitude data for the Q-output (signed), 64 registers. |

| Addr. | Name | R/W | Bit | Description | Reset | Type | Comment |
|---------|------------|-----|-------------------------|--|-------|------|--|
| 080-08F | TX_SD | R/W | 12 11 10:5 4:0 | Enable I sign switching Enable Q sign switching LUT start address Number of samples | h0000 | | The sign switching bits determine if the sign should be switched at the start of the instruction. The LUT start address is zero indexed. |
| 090-09F | TX_HOLD | R/W | 11:0 | Hold value | h0000 | | TX microcode table for user defined instructions, 16 registers. Determines how long the last sample of the LUT command shall be held. Specified in TX clock cycles. |
| 0A0 | TX_SD_D0_0 | R/W | 12 11 10:5 4:0 | Enable I sign switching Enable Q sign switching LUT start address Number of samples | h0000 | | TX microcode for first part of data-0. |
| 0A1 | TX_SD_D0_1 | R/W | 12 11 10:5 4:0 | Enable I sign switching Enable Q sign switching LUT start address Number of samples | h0000 | | TX microcode for second part of data-0. |
| 0A2 | TX_SD_D1_0 | R/W | 12 11 10:5 4:0 | Enable I sign switching Enable Q sign switching LUT start address Number of samples | h0000 | | TX microcode for first part of data-1. |
| 0A3 | TX_SD_D1_1 | R/W | 12 11 10:5 4:0 | Enable I sign switching Enable Q sign switching LUT start address Number of samples | h0000 | | TX microcode for second part of data-1. |
| 0A4 | TX_SD_N0 | R/W | 12 11 10:5 4:0 | Enable I sign switching Enable Q sign switching LUT start address Number of samples | h0000 | | TX microcode for first part of the default symbol. |
| 0A5 | TX_SD_N1 | R/W | 12 11 10:5 4:0 | Enable I sign switching Enable Q sign switching LUT start address Number of samples | h0000 | | TX microcode for second part of the default symbol. |
| 0A6 | TX_SD_RU | R/W | 12 11 10:5 4:0 | Enable I sign switching Enable Q sign switching LUT start address Number of samples | h0000 | | TX microcode for the ramp-up. This is used for the initial ramp-up as well as the ramp-up of the EOT command. |



| Addr. | Name | R/W | Bit | Description | Reset | Type | Comment |
|-------|-------------|-----|-------------------------|--|-------|------|---|
| 0A7 | TX_SD_RD | R/W | 12 11 10:5 4:0 | Enable I sign switching Enable Q sign switching LUT start address Number of samples | h0000 | | TX microcode for the ramp-down. |
| 0A8 | TX_SD_BIN_0 | R/W | 12 11 10:5 4:0 | Enable I sign switching Enable Q sign switching LUT start address Number of samples | h0000 | | TX microcode for first part of the bin-pulse. |
| 0A9 | TX_SD_BIN_1 | R/W | 12 11 10:5 4:0 | Enable I sign switching Enable Q sign switching LUT start address Number of samples | h0000 | | TX microcode for first part of the bin-pulse. |
| 0B0 | TX_H_D0_0 | R/W | 11:0 | Hold value | h0000 | | TX microcode for first part of data-0. |
| 0B1 | TX_H_D1_1 | R/W | 11:0 | Hold value | h0000 | | TX microcode for second part of data-0. |
| 0B2 | TX_H_D1_0 | R/W | 11:0 | Hold value | h0000 | | TX microcode for first part of data-1. |
| 0B3 | TX_H_D1_1 | R/W | 11:0 | Hold value | h0000 | | TX microcode for second part of data-1. |
| 0B4 | TX_H_N0 | R/W | 11:0 | Hold value | h0000 | | TX microcode for first part of the default symbol. |
| 0B5 | TX_H_N1 | R/W | 11:0 | Hold value | h0000 | | TX microcode for second part of the default symbol. |
| 0B6 | TX_H_RU | R/W | 11:0 | Hold value | h0000 | | TX microcode for the ramp-up. |
| 0B7 | TX_H_RD | R/W | 11:0 | Hold value | h0000 | | TX microcode for the ramp-down. |
| 0B8 | TX_H_BIN_0 | R/W | 11:0 | Hold value | h0000 | | TX microcode for first part of the bin-pulse. |
| 0B9 | TX_H_BIN_1 | R/W | 11:0 | Hold value | h0000 | | TX microcode for first part of the bin-pulse. |

| Addr. | Name | R/W | Bit | Description | Reset | Type | Comment |
|-------|------------|-----|---|--|-------|-------|--|
| 0C0 | TX_ENABLE | R/W | 11 10 9 8 7:6 5:4 3:2 1 0 | Bypass of Hilbert filter Hilbert filter order select Not used Not used DAC input select TX mode (Q) TX mode (I) SSB Enable Enable TX (tx_go) | h0000 | | Setup register for the TX datapath. The Hilbert filter can be switched between two orders: 1= 10th order 0= 22nd order The DAC input select can be set to the following values: 11, 10= Control output 01= Bypass interpolation filter 00= Enable interpolation filter TX mode can be set to the following values: 11= Use predistortion 10= Use output of power scaler 01= Use Hilbert transformer 00= Use Hilbert transformer and CORDIC. The enable TX signal is used for starting the TX state machine. |
| 0C1 | TX_COEFF1 | R/W | 11:0 | Hilbert coefficient 1 | h0009 | s1.10 | Used for 22nd order only, must be set to zero for the 10th order filter. |
| 0C2 | TX_COEFF3 | R/W | 11:0 | Hilbert coefficient 3 | h0017 | s1.10 | Used for 22nd order only, must be set to zero for the 10th order filter. |
| 0C3 | TX_COEFF5 | R/W | 11:0 | Hilbert coefficient 5 | h0031 | s1.10 | Used for 22nd order only, must be set to zero for the 10th order filter. |
| 0C4 | TX_COEFF7 | R/W | 11:0 | Hilbert coefficient 7 | h005f | s1.10 | |
| 0C5 | TX_COEFF9 | R/W | 11:0 | Hilbert coefficient 9 | h00c2 | s1.10 | |
| 0C6 | TX_COEFF11 | R/W | 11:0 | Hilbert coefficient 11 | h0284 | s1.10 | |
| 0C7 | TX_FREQ1 | R/W | 15:0 | CORDIC offset | h0000 | u1.18 | Frequency offset value, bit 18:3. Specified as a fraction of 2 ⁷ radians per TX clock cycle. |
| 0C8 | TX_FREQ2 | R/W | 2:0 | CORDIC offset | h0000 | | Frequency offset value, bit 2:0. Specified as a fraction of 2 ⁷ radians per TX clock cycle. |
| 0C9 | GEN_RATE | R/W | 7:0 | TX clock cycle duration | h0078 | | Specifies the TX clock cycle in 48 MHz clock cycles. |
| 0CA | TX_TO | R/W | 15:0 | Final ramp-down, hold time | h0000 | | Time to wait after the final ramp-down before the PA is disabled. Specified in 48 MHz clock cycles. |
| 0CB | TX_RU_TO | R/W | 15:0 | Initial ramp-up, hold time | h0000 | | Time to wait after initial ramp up (tag reset duration). Specified from start of ramp-up in 12 MHz clock cycles. |



| Addr. | Name | R/W | Bit | Description | Reset | Type | Comment |
|-------|---------------------------|-----|-------------|---|-------|--------------|--|
| 0CC | TX_PS_GAIN | R/W | 15:8 7:0 | Power scaler gain I Power scaler gain Q | h0000 | u1.7 u1.7 | Unity gain is h80. Unity gain for SSB operation is h9B. |
| 0CD | TX_PDIST_COEFF0 | R/W | 15:0 | Predistortion coefficient, c0 | h0000 | s6.9 | |
| 0CE | TX_PDIST_COEFF1 | R/W | 15:0 | Predistortion coefficient, c1 | h0000 | s6.9 | |
| 0CF | TX_PDIST_COEFF2 | R/W | 15:0 | Predistortion coefficient, c2 | h0000 | s6.9 | |
| 0D0 | TX_PDIST_COEFF3 | R/W | 15:0 | Predistortion coefficient, c3 | h0000 | s6.9 | |
| 0D1 | TX_PDIST_COEFF4 | R/W | 15:0 | Predistortion coefficient, c4 | h0000 | s6.9 | |
| 0D2 | TX_PDIST_COEFF5 | R/W | 15:0 | Predistortion coefficient, c5 | h0000 | s6.9 | |
| 0D3 | EOT_RU_TIME | R/W | 11:0 | CORDIC disable delay | h0000 | | Time to wait (in 48 MHz clock cycles) before recentering the carrier in SSB mode after the EOT command has been read from the TX FIFO. Observe that this time must be shorter than the RX delay in the EOT command. |
| 0D4 | BIX_MAX | R/W | 15:0 | Bin symbol period | h0000 | | Specifies the length of the bin in Class 1 ping. Specified in 48 MHz clock cycles. |
| 0D5 | PR_ASK_DELAY | R/W | 15:8 7:0 | PR-ASK delay 2 PR-ASK delay 1 | h0000 | | For delaying the txpsk_phase signal. Specified in two parts, each is specified in 48 MHz clock cycles. |
| 0D6 | PA_EN_OFFSET | R/W | 15:8 7:0 | Delay after PA enable Delay after PA buffer enable | h0000 | | Provided to give PA parts a while to settle. Specified in 48 MHz cycles. |
| 0D7 | DC_REM_DELAY | R/W | 11:0 | RX delay for C1 ping | h0000 | | Delay before enabling the digital part of the receiver and DC removal in Class 1 Ping. Specified in 48 MHz clock cycles from the start of the bit/bin ramp-up. |
| 0D8 | TXFILT_HOLD_EN_DELAY | R/W | 15:0 | | h0000 | | Delay from start of EOT command until sample and hold in the TX filter is activated. Specified in 24 MHz cycles. |
| 0D9 | TXFILT_HOLD_DISABLE_DELAY | R/W | 15:0 | | h0000 | | Delay from the end of the RX cycle until the sample and hold in the TX filter is released. Specified in 24 MHz cycles. |
| 0DA | TXFILT_HOLD_PERIOD | R/W | 15:0 | | h0000 | | Period of the refresh signal. Specified in 3 MHz cycles. The automatic refresh mechanism is disabled if the period is set to h0000. |
| 0DB | RXLO_RU_DELAY | R/W | 15:0 | rxlo_ru_delay | h0000 | | Specified in 12 MHz clock cycles |
| 0DC | RXLO_TX_DELAY | R/W | 7:0 | rxlo_tx_delay | h0000 | | Specified in 48 MHz clock cycles |

| Addr. | Name | R/W | Bit | Description | Reset | Type | Comment |
|-------|----------------|-----|--------------------------|--|-------|-------|--|
| 0DD | RXLO_EOT_DELAY | R/W | 15:0 | rxlo_eot_delay | h0000 | | Specified in 24 MHz clock cycles |
| 0DE | TXDAC_BYPASS | R/A | 7:6 5:4 3:2 0:1 | DAC Q two pole select DAC I two pole select DACDAC I select Q select | h00F0 | | 0: SD-DAC 1: Bypass DAC 2: Constant 0 3: Constant 1 |
| 0F0 | MO_TX_DATA_I | R | 12 11:0 | Enable manual override TX data I | h0000 | s1.10 | For reading the I-input of the TX data path. |
| | | W | 11:0 12 | Enable manual override Override value for TX data I | h0000 | s1.10 | For overriding the I-input of the TX data path. |
| 0F1 | MO_TX_DATA_Q | R | 12 11:0 | Enable manual override TX data Q | h0000 | s1.10 | For reading the Q-input of the TX data path. |
| | | W | 12 11:0 | Enable manual override Override value for TX data Q | h0000 | s1.10 | For overriding the Q-input of the TX data path. |
| 0F2 | MO_CORDIC_I | R | 12 11:0 | Enable manual override Hilbert transformer output I | h0000 | s1.10 | For reading the I-output of the Hilbert transformer. |
| | | W | 12 11:0 | Enable manual override Override value for the I-input to the CORDIC | h0000 | s1.10 | For overriding the I-input of the CORDIC. |
| 0F3 | MO_CORDIC_Q | R | 12 11:0 | Enable manual override Hilbert transformer output Q | h0000 | s1.10 | For reading the Q-output of the Hilbert transformer. |
| | | W | 12 11:0 | Enable manual override Override value for the Q-input to the CORDIC | h0000 | s1.10 | For overriding the Q-input of the CORDIC. |
| 0F4 | MO_DAC_I | R | 14 13:0 | Enable manual override DAC I-input | h0000 | s2.11 | For reading the I-input of the DAC. |
| | | W | 14 13:0 | Enable manual override Override value for the DAC I-input | h0000 | s2.11 | For overriding the I-input of the DAC. |
| 0F5 | MO_DAC_Q | R | 14 13:0 | Enable manual override DAC Q-input | h0000 | s2.11 | For reading the Q-input of the DAC. |
| | | W | 14 13:0 | Enable manual override Override value for the DAC Q-input | h0000 | s2.11 | For overriding the Q-input of the DAC. |



| Addr. | Name | R/W | Bit | Description | Reset | Type | Comment |
|-------|----------------|-----|--------|--------------------------------|-------|------|--|
| 0F6 | MO_FREQ_OFF_EN | R | 2 | Enable manual override | h0000 | | For reading the TX frequency offset enable bit |
| | | | 1 | Override value | | | |
| | | | 0 | TX freq. offset value | | | |
| | | W | 2 | Enable manual override | h0000 | | For overriding the TX frequency offset enable bit. |
| | | | 1 | Override value | | | |
| | | | 0 | Not used | | | |
| 0F7 | MO_RXLO_ENABLE | R | 3 | Enable Internal LO | h0000 | | |
| | | | 2 | Enable External LO | | | |
| | | | 1 | Enable MO of rxlo_enable | | | |
| | | | 0 | rxlo_enable from FSM | | | |
| | | W | 3 | Enable Internal LO | h0000 | | |
| | | | 2 | Enable External LO | | | |
| | | | 1 | Enable MO of rxlo_enable | | | |
| | | | 0 | Override value for rxlo_enable | | | |
| 100 | CTRL | R/W | 1 0 | IRQ enable Mission mode | h0000 | | Control register |
| 101 | IRQ_MASK | R/W | 11:0 | Interrupt mask | h0000 | | Masks only the interrupt pin not the interrupt status register |
| 102 | LOCK_TO | R/W | 15:0 | PLL additional settling time | h0000 | | Time to wait after the PLL has locked before entering mission mode. Specified in 48 MHz clock cycles. |
| 103 | MODE | R/W | 4 | Enable 3 MHz second LO | h0000 | | Mode settings for Indy R1000 reader chip control block. The RX data path has to be configured separately. |
| | | | 3 | Enable txpsk_phase. | | | |
| | | | 2 | ISO 18000 / Class 1 Scroll | | | |
| | | | 1 | Class 1 Ping | | | |
| | | | 0 | Not used | | | |
| 104 | REVISION | R | 3:0 | Control block revision number | h000C | | |
| 105 | T2R | R | 15:0 | Indirect address for T2R | h0000 | | |
| | R2T | W | 15:0 | Indirect address for R2T | h0000 | | |
| 106 | DP_STAT | R | 7:0 | Indirect address for DP_STAT | h0000 | | |
| | DP_CTRL | W | 7:0 | Indirect address for DP_CTRL | h0044 | | |
| 107 | ISR | R | 11:0 | Indirect address for ISR | h0000 | | Read clears all nibbles of the interrupt register. |
| 108 | MO_LOCK_DET | R | 2 | Enable manual override | h0000 | | |
| | | | 1 | Override value | | | |
| | | | 0 | Lock detect signal from FSM | | | |

| Addr. | Name | R/W | Bit | Description | Reset | Type | Comment |
|-------|--------------|-----|--|--|-------|------|---|
| | | W | 2 1 0 | Enable manual override Override value Not used | h0000 | | For overriding the lock detect signal from the FSM. |
| 109 | AUTO_READ | R/W | 12 11 10 9 8 7 6 5 4 3 2 1 0 | Auto-read of pream_mag Auto-read of rcorr_mag Auto-read WB rssi_rt_values Auto-read NB rssi_rt_values Auto-read of tx_dac_q Auto-read of tx_dac_i Auto-read of rx_dec_q Auto-read of rx_dec_i Auto-read of rx_filt_q Auto-read of rx_filt_i Auto-read of rx_ph Auto-read of ISR Auto-read of RX FIFO | h0000 | | Serial interface control. Settings 7 and 8 are sampled at 4x the GEN_RATE specified in register h0C9 |
| 10A | DIS_T2R | R/W | 1 0 | Disable T2R_D2 Disable T2R_D1 | h0000 | | Serial interface control for disabling channels. Observe that T2R_D2 must not be enabled when T2R_D1 is disabled. |
| 10B | SEED_HIGH | R/W | 15:0 | LFSR seed high word | hA5A5 | | |
| 10C | SEED_LOW | R/W | 15:0 | LFSR seed low word | h5A5A | | |
| 10D | AUX_ADC_DATA | R | 7:0 | AUX ADC Data | h0000 | | |
| 10E | CLKOUT_CTRL | R/W | 2:0 | Clock output setting | h0005 | | The clock output setting is decoded as follows: 0 = 48 MHz 1 = 24 MHz 2 = 12 MHz 3 = 6 MHz 4 = 3 MHz 5 = 1.5 MHz (default) 6 = Constant low output 7 = Constant high output |



| Addr. | Name | R/W | Bit | Description | Reset | Type | Comment | |
|-------|-------------------|-----|------------------------------|-----------------------------------|----------|--|--|-------------------------------|
| 110 | LOCK_DET_THOLD | R/W | 7:0 | PLL up/down pulse width threshold | h0000 | | The threshold for the high period of the up/down signal when the PLL is deemed unlocked. Specified in 48 MHz clock cycles. | |
| 111 | LOCK_DETECT_CNT | R/W | 15:0 | Lock detect integration time | h0000 | | Number of comparison cycles until lock detect is asserted. Specified in 48 MHz cycles. | |
| 112 | IF_TUNING_CTRL | R/W | 2:1 | Tuning speed | h0000 | | The tuning speed settings generates the following tuning rates: 0 = 100 kHz 1 = 50 kHz 2 = 25 kHz The start tuning bit is self-clearing. | |
| | | | 0 | Start tuning | | | | |
| 113 | MO_DCREM | R | 5 | Enable override (dcrem_short) | h0000 | | | |
| | | | 4 | Override value (dcrem_short) | | | | |
| | | | 3 | dcrem_short value from FSM | | | | |
| | | | 2 | Enable override (dcrem_open) | | | | |
| | | | 1 | Override value (dcrem_open) | | | | |
| | | | 0 | dcrem_open value from FSM | | | | |
| | | | W | 5 | | | | Enable override (dcrem_short) |
| | | 4 | Override value (dcrem_short) | | | | | |
| | | 3 | Not used | | | | | |
| | | 2 | Enable override (dcrem_open) | | | | | |
| | | 1 | Override value (dcrem_open) | | | | | |
| | | 0 | Not used | | | | | |
| | | 114 | CLK_DBL_MO | R/W | 8 7:0 | Enable manual override Override value for clock doubler | h0000 | |
| | | 115 | CLK_DBL_VALUE | R | 7:0 | Clock doubler value | h0000 | |
| 200 | RX_MAX | R/W | 11:0 | Expected number of bits | h0000 | | The number of bits that will be received from the tag. If this is set to zero then 212-1 bits will be received. | |
| 202 | PREAM_SEARCH_WAIT | R/W | 15:0 | Preamble search delay | h0000 | | This is the delay between the start of the digital receiver and when the preamble can be found. Specified in 3 MHz clock cycles. | |

| Addr. | Name | R/W | Bit | Description | Reset | Type | Comment |
|-------|-----------------|-----|------------------|--|-------|------|--|
| 203 | RX_TO | R/W | 15:0 | Receiver time-out | h0000 | | The time after the preamble search starts when the receiver will time-out. Specified in 3 MHz clock periods. |
| 204 | MO_RX_START | R | 1 0 | Enable manual override Value of rx_start from FSM | h0000 | | |
| | | W | 1 0 | Enable manual override Override value for rx_start | h0000 | | For starting the digital part of the receiver manually. |
| 206 | IFLNA_TH_CNT | R/W | 15:0 | IF LNA too high threshold | h0000 | | IF LNA too high count. This determines how many 3 MHz clock cycles the too high signal from the peak detector needs to be asserted before asserting if_lna_too_high. |
| 207 | IFLNA_TL_CNT | R/W | 15:0 | IF LNA too low threshold | h0000 | | This determines how many 3 MHz clock cycles the too low signal from the peak detector needs to be asserted before asserting if_lna_too_low. |
| 208 | IFLNA_RESET_CNT | R/W | 15:0 | IF LNA peak detector reset interval | h0000 | | The number of 3 MHz clock cycles between the reset pulses to the IF LNA peak detector. |
| 209 | ADC_OD_THRES | R/W | 4:0 | ADC input overdrive threshold | h000F | | |
| 210 | DEC_ENABLE | R/W | 1 0 | Enable decimate by 16 Enable programmable decimation | h0000 | | Bit 0 needs to be set in order for the setting in register h211 to take effect. |
| 211 | DEC_MUX_SEL | R/W | 1:0 | Decimation selection | h0000 | | Selection of decimation order: 0 = Decimate by 16 1 = Decimate by 32 2 = Decimate by 64 3 = Decimate by 128 |
| 212 | MO_RX_DEC_I | R | 15:0 | I-output of decimation chain | h0000 | | For reading the I-output of the decimation chain (sign extended to 16 bits). |
| | | W | 15 14 13:0 | Not used Enable manual override Override value for decimation output I | h0000 | | For overriding the I-output of the decimation chain. |
| 213 | MO_RX_DEC_Q | R | 15:0 | Q-output of decimation chain | h0000 | | For reading the Q-output of the decimation chain (sign extended to 16 bits). |
| | | W | 15 14 13:0 | Not used Enable manual override Override value for decimation output Q | h0000 | | For overriding the Q-output of the decimation chain. |



| Addr. | Name | R/W | Bit | Description | Reset | Type | Comment |
|---------|---------------|-----|------|--------------------------------|-------|-------|---|
| 214 | MO_RXDEC_STAT | R | 1 | Status of manual override (Q) | h0000 | | This is the read back register for the enable manual override defined in registers h212 and h213. |
| | | | 0 | Status of manual override (I) | | | |
| 220 | RX_FIR_EN | R/W | 0 | Enable RX FIR filter | h0000 | | |
| 221 | RX_FIR_LENGTH | R/W | 2:0 | Select RX FIR filter length | h0000 | | Sets the length of the receive FIR filter: 0 = 36 taps 1 = 42 taps 2 = 48 taps 3 = 54 taps 4 = 60 taps 5 = 66 taps 6 = 72 taps |
| 222-245 | CF_COEFF | R/W | 11:0 | RX FIR filter coefficients | h0000 | | Coefficients for the receive FIR channel filter. The coefficients are symmetric, i.e., c0=c71. 36 registers, h222 specifies c0. For filters shorter than 72 taps, only the coefficients used (c0 to c#taps-1) must be specified. |
| 250 | MO_RX_IIR | R | 6 | Enable manual override | h0000 | | |
| | | | 5 | Enable RX IIR filter | | | |
| | | | 4 | rx_iir_hold signal from FSM | | | |
| | | | 3:0 | Number of bits to hold IIR | | | |
| | | W | 6 | Enable manual override | h0000 | | The IIR filter output is set to zero whenever the filter is disabled. |
| | | | 5 | Enable RX IIR filter | | | |
| | | | 4 | Override value of rx_iir_hold | | | The FSM sets rx_iir_hold high when the remaining bits to be received is less than or equal to rx_iir_hold_bits. |
| | | | 3:0 | Number of bits to hold IIR | | | |
| 251 | COEFF_A1_1 | R/W | 0 | Bit 16 of IIR coefficient a1 | h0000 | s1.15 | Denominator coefficient. |
| 252 | COEFF_A1_2 | R/W | 15:0 | Bit 15:0 of IIR coefficient a1 | h0000 | | Denominator coefficient. |
| 253 | COEFF_A2_1 | R/W | 0 | Bit 16 of IIR coefficient a2 | h0000 | s1.15 | Denominator coefficient. |
| 254 | COEFF_A2_2 | R/W | 15:0 | Bit 15:0 of IIR coefficient a2 | h0000 | | Denominator coefficient. |

| Addr. | Name | R/W | Bit | Description | Reset | Type | Comment |
|-------|----------------|-----|------------|--|-------|-------|--|
| 255 | COEFF_B1 | R/W | 3:0 | IIR coefficient b1 | h0000 | | Numerator coefficient. This value is not used anywhere. Inside the IIR filter b1 is hard-coded to 2. |
| 256 | COEFF_S1_1 | R/W | | Bit 16 of IIR scale factor s1 | h0000 | s1.15 | |
| 257 | COEFF_S1_1 | R/W | | Bit 15:0 of IIR scale factor s1 | h0000 | | |
| 260 | RX_FILTER_SEL | R/W | 0 | Bypass RX channel filters | h0000 | | 0 = Include filters. 1 = No filtering. |
| 261 | MO_RX_FILT_I | R | 15:0 | RX filter I-output | h0000 | | The output value is sign extended to 16 bits. |
| | | W | 15 | Not used | h0000 | | |
| | | | 14 13:0 | Enable manual override Override value of RX filter I-output | | | |
| 262 | MO_RX_FILT_Q | R | 15:0 | RX filter Q-output | h0000 | | The output value is sign extended to 16 bits. |
| | | W | 15 | Not used | h0000 | | |
| | | | 14 13:0 | Enable manual Override value of RX filter Q-output | | | |
| 263 | MO_RXFILT_STAT | R | 1 | Status of manual override (Q) | b0000 | | This is the read back register for the enable manual override defined in registers h262 and h263. |
| | | | 0 | Status of manual override (I) | | | |
| 270 | RX_PH_RECOV_EN | R/W | 10:4 | Fixed phase rotation value | h0000 | u0.7 | Bit 0 enables/disables the phase recovery. If bit 1 is set the rotation is fixed and determined by bits 10:4. The rotation is specified as a fraction of 2 ⁷ . |
| | | | 3:2 | Not used | | | |
| | | | 1 | Enable fixed reg-based rotation | | | |
| | | | 0 | Enable phase recovery | | | |
| 271 | REG_KS1 | R/W | 2:0 | Phase recovery prop. gain | h0000 | | Proportional gain of the phase recovery: 0 = 8 * 2 ⁻¹⁰ 1 = 16 * 2 ⁻¹⁰ 2 = 32 * 2 ⁻¹⁰ 3 = 64 * 2 ⁻¹⁰ 4 = 128 * 2 ⁻¹⁰ 5 = 256 * 2 ⁻¹⁰ 6 = 512 * 2 ⁻¹⁰ 7 = 1 |



| Addr. | Name | R/W | Bit | Description | Reset | Type | Comment |
|-------|------------|-----|--------------------------------|---|-------|------|---|
| 272 | REG_KS2 | R/W | 2:0 | Phase recovery intg. gain | b0000 | | Integrator gain of phase recovery: 0 = 1 * 2 ⁻¹⁰ 1 = 2 * 2 ⁻¹⁰ 2 = 4 * 2 ⁻¹⁰ 3 = 8 * 2 ⁻¹⁰ 4 = 16 * 2 ⁻¹⁰ 5 = 32 * 2 ⁻¹⁰ 6 = 64 * 2 ⁻¹⁰ 7 = 128 * 2 ⁻¹⁰ |
| 273 | MO_RX_PH | R/W | 0 | Enable manual override | h0000 | | Enable manual override of phase recovery output. |
| 274 | RX_PH | R | 15:0 | Phase recovery output | h0000 | | |
| | | W | 15:0 | Override value of phase recovery output | h0000 | | |
| 280 | RSSI_START | R | 3 | Enable manual start of NB RSSI | h0000 | | |
| | | | 2 | NB RSSI start value from FSM | | | |
| | | | 1 | Enable manual start of WB RSSI | | | |
| | | | 0 | WB RSSI start value from FSM | | | |
| | | W | 3 | Enable manual start of NB RSSI | | | The start bits are self-clearing. |
| | | | 2 | Manual start of NB RSSI | | | |
| | | 1 | Enable manual start of WB RSSI | | | | |
| | | 0 | Manual start of WB RSSI | | | | |

| Addr. | Name | R/W | Bit | Description | Reset | Type | Comment |
|-------|----------------|-----|---------------------------------|---|-------|------|---|
| 281 | RSSI_AVERAGING | R/W | 12:10 9:7 6 5:3 2:0 | Averaging of RT NB RSSI Averaging of RT WB RSSI Enable real-time RSSI Averaging of NB RSSI Averaging of WB RSSI | h0000 | | <p>The normal narrow-band RSSI averaging can assume the following values:</p> <p>0 = 8 samples. 1 = 16 samples. 2 = 32 samples. 3 = 64 samples. 4 = 128 samples. 5 = 256 samples. 6 = 512 samples. 7 = 1024 samples.</p> <p>The normal wide-band RSSI averaging can assume the following values:</p> <p>0 = 64 samples. 1 = 128 samples. 2 = 256 samples. 3 = 512 samples. 4 = 1024 samples. 5 = 2048 samples. 6 = 4096 samples 7 = 8192 samples.</p> |
| 282 | RSSI_VALUES | R | 15:8 7:0 | Narrow-band RSSI value Wide-band RSSI value | h0000 | | |
| 283 | RSSI_RT_VALUES | R | 15:8 7:0 | Real-time NB RSSI value Real-time WB RSSI value | h0000 | | |
| 284 | AUX_ADC_START | R | 5 4 3:0 | Enable manual start Start signal from FSM AUX ADC mux selection | h0000 | | |
| | | W | 5 4 3:0 | Enable manual start Manual start AUX ADC mux selection | h0000 | | For starting an AUX ADC measurement manually. The start bit is self-clearing. |
| 290 | MO_MATCH_FILT | R | 13 12:10 9:2 1 0 | Enable manual override Value of max_idx Value of max_mag Value of rclk_match_filt Value of pream_found | h0000 | | |



| Addr. | Name | R/W | Bit | Description | Reset | Type | Comment |
|-------|---------------|-----|------------------------------|--|-------|----------------|--|
| | | W | 13 12:10 9:2 1 0 | Enable manual override Override value of max_idx Override value of max_mag Override value of rclk_match_filt Override value of pream_found | h0000 | | |
| 291 | DEMOD_ENABLE | R/W | 1 0 | Enable ISO demodulator Enable ISO demod clk generation | h0000 | | |
| 292 | SFILT_COEFF_1 | R/W | 15:8 7:0 | Smoothing filter coefficient c2 Smoothing filter coefficient c1 | h0000 | s-1.8 s-1.8 | The coefficients are numbered from c1 to c16 |
| 293 | SFILT_COEFF_2 | R/W | 15:8 7:0 | Smoothing filter coefficient c4 Smoothing filter coefficient c3 | h0000 | s-1.8 s-1.8 | |
| 294 | SFILT_COEFF_3 | R/W | 15:8 7:0 | Smoothing filter coefficient c6 Smoothing filter coefficient c5 | h0000 | s-1.8 s-1.8 | |
| 295 | SFILT_COEFF_4 | R/W | 15:8 7:0 | Smoothing filter coefficient c8 Smoothing filter coefficient c7 | h0000 | s-1.8 s-1.8 | |
| 296 | SFILT_COEFF_5 | R/W | 15:8 7:0 | Smoothing filter coefficient c10 Smoothing filter coefficient c9 | h0000 | s-1.8 s-1.8 | |
| 297 | SFILT_COEFF_6 | R/W | 15:8 7:0 | Smoothing filter coefficient c12 Smoothing filter coefficient c11 | h0000 | s-1.8 s-1.8 | |
| 298 | SFILT_COEFF_7 | R/W | 15:8 7:0 | Smoothing filter coefficient c14 Smoothing filter coefficient c13 | h0000 | s-1.8 s-1.8 | |
| 299 | SFILT_COEFF_8 | R/W | 15:8 7:0 | Smoothing filter coefficient c16 Smoothing filter coefficient c15 | h0000 | s-1.8 s-1.8 | |
| 2A0 | DRATE_ENABLE | R/W | 1 0 | Enable data rate correction Hold correction on preamble found | h0000 | | |

| Addr. | Name | R/W | Bit | Description | Reset | Type | Comment |
|---------|-------------------------|-----|----------------------|--|-------|------|--|
| 2A1-2AB | RCORR_TICKS | R/W | 13:0 | Clock rates of rate correlators | h0000 | | Number of 48 MHz clock ticks per oversampled demodulator clock period. The value is scaled with 2-4. |
| 2B1-2BB | RCORR_LUT | R/W | 13:0 | Tick compensation LUT | h0000 | | |
| 2BC | RCORR_MAG | R | 6:0 | Maximum magnitude of the rate estimation correlators | h0000 | | This register has auto-read capabilities. |
| 2BD | DRATE_CTRL | R/W | 8 7 6:2 1:0 | Enable abs value in rate est restart Enable median filter in restart Peak hold counter Rate estimation coefficient select | h0000 | | The modes of the rate estimation is: 0 = 1111 1111 0000 0000 (FM0) 1 = 1111 0000 1111 0000 (M=2) 2 = 1100 1100 1100 1100 (M=4 and M=8) 3 = 1010 1010 1010 1010 (Spare) |
| 2BE | DRATE_THRES | R/W | 15:8 6:0 | Rate estimator restart threshold Rate correction threshold | hFF00 | | If the rate estimator restart threshold is set to hFF the restart mechanism is disabled. |
| 2BF | DRATE_CNT_THRES | R/W | 15:8 7:0 | Above count threshold Below count threshold | h0000 | | The number of samples above/below the threshold required to set/ reset rate est. flag. |
| 2C0 | FIFO_DELAY_SEL | R/W | 2:0 | Delay select | b0000 | | Delay between rate estimator and the rest of the demodulator: 0 = 0 samples. 1 = 32 samples. 2 = 64 samples. 3 = 96 samples. 4 = 128 samples. 5 = 160 samples. 6 = 192 samples. |
| 2C1 | DEMOD_DEFAULT_NUM_TICKS | R/W | 13:0 | Ticks per oversampled clock | h0000 | s9.4 | Number of 48 MHz clock ticks per oversampled demodulator clock period. |
| 2C2 | GAD_INT_GAIN_PREAM | R/W | 9:0 | Proportional gain, before the preamble is found | h0000 | s3.6 | Proportional timing recovery gain before the preamble is found. |
| 2C3 | GAD_INT_GAIN | R/W | 9:0 | Integrator gain, before the preamble is found | h0000 | s1.8 | Integrator timing recovery gain before the preamble is found. |
| 2C4 | GAD_PROP_GAIN_PREAM | R/W | 9:0 | Proportional gain, after the preamble is found | h0000 | s3.6 | Proportional timing recovery gain after the preamble is found. |
| 2C5 | GAD_PROP_GAIN | R/W | 9:0 | Integrator gain, after the preamble is found | h0000 | s1.8 | Integrator timing recovery gain after the preamble is found. |



| Addr. | Name | R/W | Bit | Description | Reset | Type | Comment |
|-------|-----------------------|-----|---------|--|-------|------|--|
| 2C6 | GARDNER_CTRL | R/W | 4 | En GAD when rate est. has locked | h0000 | | When reset is enabled the loop filter and/or the clock generation is reset when the preamble is found. Bit 0 must always be zero for proper operation. |
| | | | 3 | Reset GAD with rate estimator | | | |
| | | | 2 | Enable median filter in GAD | | | |
| | | | 1 | Enable reset of GAD loop filter | | | |
| | | | 0 | (Enable clock generation reset) | | | |
| 2D0 | MO_BEGIN_PREAM_SEARCH | R | 2 | Enable manual override | h0000 | | |
| | | | 1 | Override value for begin_pream_search | | | |
| | | | 0 | begin_pream_search from FSM | | | |
| | | W | 2 | Enable manual override | | | Enables override of begin_pream_search. |
| | | | 1 | Override value for begin_pream_search | | | |
| | | | 0 | Not used | | | |
| 2D1 | PREAM_CTRL | R/W | 13:8 | Preamble threshold | h0000 | | The type of preamble can be set to the following: 0 = ISO FM0. 1 = ISO Miller. 2 = C1G1 Scroll ID. 3 = ISO FM0. The matched filter can be set to the following: 0 = ISO FM0. 1 = ISO Miller. 2 = C1G1 Scroll ID. 3 = ISO FM0. |
| | | | 7:4 | Not used | | | |
| | | | 31:0: 2 | Select preamble Select matched filter | | | |
| 2D2 | MILLER_CTRL | R/W | 10 | Miller subcarrier filter selection | h0000 | | |
| | | | 9:6 | Miller M value | | | |
| | | | 5:2 | Sub-carrier alignment delay | | | |
| | | | 1 | Enable Miller clock | | | |
| | | | 0 | Enable Miller sub-carrier removal | | | |
| 2D3 | SFILT_OUTPUT | R | 7:0 | Smoothing filter output | h0000 | | Testpoint |
| 2D4 | DRATE_NCO_INPUT | R | 13:0 | Data rate est. input to NCO | h0000 | | Testpoint |
| 2D5 | GAD_NCO_INPUT | R | 10:0 | GAD input to NCO | h0000 | | Testpoint |

| Addr. | Name | R/W | Bit | Description | Reset | Type | Comment |
|-------|-------------------|-----|------|---|-------|-------|--|
| 2D6 | PREAM_MAG | R | 6:0 | Magnitude of the preamble correlator | h0000 | | This register has auto-read capabilities. |
| 2D7 | PREAM_MAG_PEAK | R | 6:0 | Peak magnitude of the preamble correlator | h0000 | | Reset at the beginning of each RX slot. Once the preamble is found this register will hold the peak preamble correlator value. This register can be used to evaluate the signal quality. |
| 2D8 | MILLER_COEFF_A1_1 | R/W | 0 | Bit 16 of IIR coefficient a1 | h0000 | s1.15 | |
| 2D9 | MILLER_COEFF_A1_2 | R/W | 15:0 | Bit 15:0 of IIR coefficient a1 | h0000 | | |
| 2DA | MILLER_COEFF_A2_1 | R/W | 0 | Bit 16 of IIR coefficient a2 | h0000 | s1.15 | |
| 2DB | MILLER_COEFF_A2_2 | R/W | 15:0 | Bit 15:0 of IIR coefficient a2 | h0000 | | |
| 2DC | MILLER_COEFF_S1_1 | R/W | 0 | Bit 16 of IIR coefficient s1 | h0000 | s1.15 | |
| 2DD | MILLER_COEFF_S1_2 | R/W | 15:0 | Bit 15:0 of IIR coefficient s1 | h0000 | | |
| 300 | PING_EN | R/W | 0 | Enable ping demodulator | h0000 | | |
| 301 | TSW_CNT | R/W | 8:0 | Tag setup window sample delay | h0000 | | Determines when the power of the tag setup window is sampled. Specified from the start of the digital receiver expressed in demodulator sample periods. |
| 302 | PWR_TH | R/W | 4:0 | Relative power threshold | h0000 | | The relative power threshold of the C1 ping demodulator. The reference power is the power sampled in the tag setup window. |
| 303 | BIT_TH | R/W | 10:0 | Bit slicing level | h0000 | | Bit slicing level for the C1 ping demodulator. Specified in 48 MHz clock cycles. |



| Addr. | Name | R/W | Bit | Description | Reset | Type | Comment |
|-------|----------|-----|----------|------------------------|-------|------|---|
| 400 | ANA_EN1 | R | 14 | lna_e | h0000 | | lo_e and lo_poly_e can only be read-back through this register. The behavior of these signals is controlled through registers h0F7 and h0DB-h0DD. |
| | | | 13 | mix_lo_en | | | |
| | | | 12 | lo_e | | | |
| | | | 11 | lo_poly_en | | | |
| | | | 10 | rflna_pdet_e | | | |
| | | | 9 | rf_pdet_e | | | |
| | | | 8 | lo_pdet_e | | | |
| | | | 7 | iflna_e | | | |
| | | | 6 | iflna_pdet_e | | | |
| | | | 5 | Not used | | | |
| | | | 4 | iffilt_e | | | |
| | | | 3 | tune_e | | | |
| | | | 2 | ifagc_e | | | |
| | | | 1 | rxadc_e | | | |
| | | 0 | txfilt_e | | | | |
| | | W | 14 | lna_e | h0000 | | Analog enable signals. lna_e: Enable RF LNA mix_lo_e: Enable RX mixer LO rflna_pdet_e: Enable RF LNA peak detector lo_pdet_e: Enable LO peak detector iflna_e: Enable IF LNA iflna_pdet_e: Enable IF LNA peak detector iffilt_e: Enable IF filter tune_e: Enable analog filter tuning block ifagc_e: Enable IF AGC rxadc_e: Enable RX ADC txfilt_e: Enable TX filter |
| | | | 13 | mix_lo_en | | | |
| | | | 12 | Not used | | | |
| | | | 11 | Not used | | | |
| | | | 10 | rflna_pdet_e | | | |
| | | | 9 | rf_pdet_e | | | |
| | | | 8 | lo_pdet_e | | | |
| | | | 7 | iflna_e | | | |
| | | | 6 | iflna_pdet_e | | | |
| | | | 5 | Not used | | | |
| | | | 4 | iffilt_e | | | |
| | | | 3 | tune_e | | | |
| | | | 2 | ifagc_e | | | |
| 1 | rxadc_e | | | | | | |
| 0 | txfilt_e | | | | | | |
| 401 | ANA_EN2 | R | 9 | Enable manual override | h0000 | | Analog enable signals and manual override of PA signals. txlo_div_e: Enable IQ divider txlo_i_e: Enable TX LO I txlo_q_e: Enable TX LO Q txmix_ssb_e: Enable SSB mode txmix_pski_e: Enable I modulator txmix_pskq_e: Enable Q modulator |
| | | | 8 | pa_buffer_e from FSM | | | |
| | | | 7 | pa_driver_e from FSM | | | |
| | | | 6 | pa_pa_e from FSM | | | |
| | | | 5 | txlo_div_e | | | |
| | | | 4 | txlo_i_e | | | |
| | | | 3 | txlo_q_e | | | |
| | | | 2 | txmix_ssb_e | | | |
| | | | 1 | txmix_pski_e | | | |
| | | | 0 | txmix_pskq_e | | | |

| Addr. | Name | R/W | Bit | Description | Reset | Type | Comment |
|-------|---------|-----|-----|--------------------------------|-------|------|---|
| | | W | 9 | Enable manual override | h0000 | | |
| | | | 8 | Manual override of pa_buffer_e | | | |
| | | | 7 | Manual override of pa_driver_e | | | |
| | | | 6 | Manual override of pa_pa_e | | | |
| | | | 5 | txlo_div_e | | | |
| | | | 4 | txlo_i_e | | | |
| | | | 3 | txlo_q_e | | | |
| | | | 2 | txmix_ssb_e | | | |
| | | | 1 | txmix_pski_e | | | |
| | | | 0 | txmix_pskq_e | | | |
| 402 | ANA_EN3 | R/W | 9 | dac1_e | h0000 | | Analog enable signals. |
| | | | 8 | dac0_e | | | dac1_e: Enable AUX DAC 1 |
| | | | 7 | modbuf_e | | | dac0_e: Enable AUX DAC 0 |
| | | | 6 | pll_ne | | | modbuf_e: Enable modulation output buffer |
| | | | 5 | pll_re | | | pll_ne: Enable PLL N divider |
| | | | 4 | pll_pdcpe | | | pll_re: Enable PLL R divider |
| | | | 3 | vco_e | | | pll_pdcpe: Enable PLL PD and CP. |
| | | | 2 | vco_detector_e | | | vco_e: Enable VCO |
| | | | 1 | vco_buffert_e | | | vco_detector_e: Enable VCO detector |
| | | | 0 | vco_divider_e | | | vco_buffert_e: Enable VCO buffer |
| | | | | | | | vco_divider_e: Enable VCO divider |



| Addr. | Name | R/W | Bit | Description | Reset | Type | Comment |
|-------|-----------|-----|-------|-----------------|-------|------|---|
| 410 | ANA_CTRL1 | R/W | 13:12 | iflنا_impedance | h0000 | | Analog control signals. |
| | | | 11:10 | lnا_bias | | | iflنا_impedance settings: |
| | | | 9:6 | mix_lo_bias | | | 0 = 10 kOhm |
| | | | 5:4 | iflنا_gain | | | 1 = 5 kOhm |
| | | | 3:2 | iflنا_pdet_hi | | | 2 = 3.3 kOhm |
| | | | 1:0 | iflنا_pdet_lo | | | 3 = 2.5kOhm |
| | | | | | | | lnا_bias setting: |
| | | | | | | | 1 = low gain mode LNA |
| | | | | | | | 0 = high gain mode LNA |
| | | | | | | | Default setting for mix_lo_bias is 10. |
| | | | | | | | The iflنا_gain setting generates the following gains: |
| | | | | | | | 0 = 24 dB |
| | | | | | | | 1 = 18 dB |
| | | | | | | | 3 = 12 dB |
| | | | | | | | The iflنا_pdet_lo setting generates the following thresholds: |
| | | | | | | | 0 = 50 mV |
| | | | | | | | 1 = 100 mV |
| | | | | | | | 2 = 200 mV |
| | | | | | | | 3 = 400 mV |
| | | | | | | | The iflنا_pdet_hi setting generates the following thresholds: |
| | | | | | | | 0 = 200 mV |
| | | | | | | | 1 = 600 mV |
| | | | | | | | 2 = 1.0 V |
| | | | | | | | 3 = 1.2 V |

| Addr. | Name | R/W | Bit | Description | Reset | Type | Comment |
|-------|-----------|-----|-----------------------|--|-------|------|--|
| 411 | ANA_CTRL2 | R/W | 15:8 7 6:1 0 | lfina_dcoffset iffilt_bp iffilt_cap iffilt_iqswap | h0000 | | <p>Analog control signals.</p> <p>lfina_dcoffset settings:</p> <p>0 = 0 mV I channel diff. offset 1 = 10 mV I channel diff. offset 2 = 20 mV I channel diff. offset 3 = 30 mV I channel diff. offset 4 = -10 mV I channel diff. offset 8 = -20 mV I channel diff. offset 12 = -30 mV I channel diff. offset 16 = 10 mV Q channel diff. offset 32 = 20 mV Q channel diff. offset 48 = 30 mV Q channel diff. offset 64 = -10 mV Q channel diff. offset 128 = -20 mV Q channel diff. offset 192 = -30 mV Q channel diff. offset</p> <p>iffilt_bp changes the RX filter from low-pass mode to band-pass mode.</p> <p>iffilt_cap controls the bandwidth of the RX filter.</p> <p>iffilt_iqswap swaps the I/Q signals at the input of the RX filter.</p> |
| 412 | ANA_CTRL3 | R/W | 11:6 5:2 1:0 | tune_r ifagc_gain ifagc_lim | h0E4C | | <p>Analog control signals.</p> <p>The ifagc_gain setting generates the following gain values:</p> <p>0 = -12 dB 4 = -6 dB 6 = 0 dB 7 = 6 dB</p> <p>The ifagc_lim setting generates the following clipping levels:</p> <p>0 = 500 mV 1 = 280 mV 2 = 180 mV 3 = 140 mV</p> |



| Addr. | Name | R/W | Bit | Description | Reset | Type | Comment |
|-------|-----------|-----|--------------------------------------|--|-------|------|---|
| 413 | ANA_CTRL4 | R/W | 13 12 11 10:9 8:6 5:0 | rxadc_lime rxadc_clkinv rxadc_pr txfilt_2p txfilt_gain txfilt_cap | h0304 | | <p>Analog control signals.</p> <p>rxadc_lime enables the limiting function in the ADC.</p> <p>rxadc_clkinv enables triggering on the falling edge of the clock instead of rising.</p> <p>rxadc_pr enables the dithering function.</p> <p>The txfilt_2p setting enables the TX-filter 2-pole mode.</p> <p>txfilt_gain default setting is 3.</p> <p>txfilt_cap controls the bandwidth of the TX filter.</p> |
| 414 | ANA_CTRL5 | R/W | 12:10 9:7 6:3 2:0 | txlo_bias txmix_gain txmix_pwr txmix_bias | h0000 | | <p>Analog control signals.</p> <p>txlo_bias control bias of the LO buffer, default setting is 3.</p> <p>txmix_gain control V2I gain, default setting is 3.</p> <p>txmix_pwr setting controls the mixer gain:</p> <p>2 = -20 dB</p> <p>3 = -18 dB</p> <p>8 = -12 dB</p> <p>11 = -10 dB</p> <p>txmix_bias has default setting 2.</p> |
| 415 | ANA_CTRL6 | R/W | 12:9 8:3 2:0 | pa_ssb pa_power pa_in_match | h0000 | | <p>Analog control signals.</p> <p>pa_ssb sets different operation modes for the PA:</p> <p>15 = Linear mode</p> <p>0 = Non-linear mode</p> <p>pa_power controls the gain in linear mode:</p> <p>3 = 13 dB</p> <p>31 = 17 dB</p> <p>pa_in_match sets the mixer load center frequency, default setting is 4.</p> |
| 416 | ANA_CTRL7 | R/W | 14:10 9:5 4:0 | pa_mid_match pa_bufbias pa_drvbias | h0000 | | <p>Analog control signals.</p> <p>pa_mid_match sets the PA driver load center frequency, default setting is 16.</p> <p>pa_bufbias sets the PA buffer bias, default setting is 7.</p> <p>pa_drvbias sets the PA driver bias, default setting is 7.</p> |

| Addr. | Name | R/W | Bit | Description | Reset | Type | Comment |
|-------|------------|-----|-------------------------------|---|-------|------|--|
| 417 | ANA_CTRL8 | R/W | 11:8 7:5 4:0 | vco_bias vco_band pa_pabias | h0000 | | Analog control signals. vco_bias setting: 0 = Minimum current 15 = Maximum current vco_band setting: 0 = Maximum frequency 7 = Minimum frequency pa_pabias sets the bias of the PA output stage, default setting in SSB mode is 16 and default setting in PSK is 7. |
| 418 | ANA_CTRL9 | R/W | 15:0 | pll_n | h0E4C | | Analog control signals. pll_n is the divider ratio of the N-divider in the PLL. |
| 419 | ANA_CTRL10 | R/W | 13:5 4 3:2 1:0 | pll_r Not used pll_inv Not used | h0000 | | Analog control signals. pll_r is the divider ratio of the R-divider in the PLL. pll_inv setting: 0 = test mode 1 = normal mode 2 = inverted feedback loop |
| 41A | ANA_CTRL11 | R/W | 15:8 7:0 | dac1_data dac0_data | h0000 | | Analog control signals. Input value to AUX DAC 1 and 0 respectively. |
| 41B | SPARE_OUT | R/W | 15:0 | Spare output | h0000 | | |
| 41C | ANA_CTRL12 | R | 1 0 | Enable MO of sample and hold. txfilt_hold from FSM | h0000 | | |
| | | W | 1 0 | Enable MO of sample and hold. txfilt_hold override value | h0000 | | |
| 420 | ANA_INPUT1 | R | 10 9 8:3 2 1 0 | vco_amp_hi vco_amp_lo tune_c tune_stop iflna_amp_hi iflna_amp_lo | | | Analog input signals. vco_amp_hi: VCO amplitude too high vco_amp_lo: VCO amplitude too low tune_c: C value from filter tuning machine tune_stop: Stop signal from filter tuning machine iflna_amp_hi: IF LNA amplitude too high iflna_amp_lo: IF LNA amplitude too low |



| Addr. | Name | R/W | Bit | Description | Reset | Type | Comment |
|-------|-------------|-----|--|--|-------|------|---|
| 421 | ANA_INPUT2 | R | 7:0 | Chip revision | | | Indy R1000 reader chip revision. |
| 422 | SPARE_IN | R | 15:0 | Spare input | | | |
| 430 | ANA_TEST1 | R/W | 9 8 7 6 5 4 3 2 1 0 | pll_test_up pll_test_down iflna_itest iflna_qtest ifagc_iitest ifagc_qitest ifagc_iouttest ifagc_qouttest txfilt_itest txfilt_qtest | | | <p>Analog test signals.</p> <p>pll_test_up: Set PLL charge pump up</p> <p>pll_test_down: Set PLL charge pump down</p> <p>iflna_itest: Enable IF LNA test I</p> <p>iflna_qtest: Enable IF LNA test Q</p> <p>ifagc_iitest: Enable IF AGC input test I</p> <p>ifagc_qitest: Enable IF AGC input test Q</p> <p>ifagc_iouttest: Enable IF AGC output test I</p> <p>ifagc_qouttest: Enable IF AGC output test Q</p> <p>txfilt_itest: Enable TX filter test I</p> <p>txfilt_qtest: Enable TX filter test Q</p> |
| 431 | ANA_TEST2 | R/W | 1 0 | adc_test atest_e | | | <p>Analog test signals</p> <p>adc_test: Enables test feedback of AUX ADC</p> <p>atest_e: Enable analog test bus</p> |
| 500 | DTEST_C_TRL | R/W | 15:10 9:4 3 2 1 0 | DTEST1 mux select DTEST0 mux select DTEST1 DTEST0 DTEST1 pin output enable DTEST0 pin output enable | | | The mux select signals are defined in Table 9 3. |

7 Performance Characteristics - Preliminary

Performance characteristics include the following:

- [Receiver Compression Point](#)
- [RF to IF Conversion Gain and Gain Flatness](#)
- [Carrier Settling Time](#)
- [Rx Sensitivity Testing](#)
- [Transmit Output Spectral Testing](#)
- [Gain Control Resolution and Dynamic Range](#)
- [ADC Testing](#)
- [Aux. DAC Testing](#)

7.1 Receiver Compression Point

A standard compression point test was performed by applying a 901 MHz signal at the input of the mixer with a 900 MHz local frequency to produce a 1 MHz baseband at the output. The amplitude of the 901 MHz signal is increased and the output compression is observed. This process was repeated over frequency and high-low gain modes. The reported compression point is referenced to the input power.

Recorded values are input power levels corresponding to an output compression of 1 dB.

Table 23: Receiver Compression Point

| | 860 MHz | 900 MHz | 960 MHz |
|-----------------------------|---------|---------|---------|
| Low gain internal LO | 13 dBm | 14 dBm | 14 dBm |
| Low gain external LO 0 dBm | 14 dBm | 14 dBm | 14 dBm |
| Low gain external LO 5 dBm | 14 dBm | 14 dBm | 14 dBm |
| Low gain external LO 10 dBm | 14 dBm | 14 dBm | 14 dBm |
| High gain internal LO | 8 dBm | 9 dBm | 9 dBm |
| High gain external 0 dBm | 9 dBm | 10 dBm | 9 dBm |
| High gain external 5 dBm | 9 dBm | 10 dBm | 9 dBm |
| High gain external 10 dBm | 9 dBm | 10 dBm | 9 dBm |

7.2 RF to IF Conversion Gain and Gain Flatness

A standard conversion gain measurement was performed by applying a 900.1 MHz signal at the input of the mixer with a 900 MHz local frequency to produce a 100 KHz baseband at the output. The IF LNA was included in the gain measurement. The amplitude of the 900.1 MHz signal is set to -30dBm to keep the IF output in a linear range.

Table 24: Gain at 100 KHz IF (dB)

| | 860 MHz | 900 MHz | 960 MHz |
|-----------------------------|---------|---------|---------|
| Low gain internal LO | 21 | 21 | 21 |
| Low gain external LO 0 dBm | 21 | 21 | 21 |
| Low gain external LO 5 dBm | 21 | 21 | 21 |
| Low gain external LO 10 dBm | 21 | 21 | 21 |
| High gain internal LO | 26 | 26 | 26 |
| High gain external 0 dBm | 26 | 26 | 26 |
| High gain external 5 dBm | 26 | 26 | 26 |
| High gain external 10 dBm | 26 | 26 | 26 |

7.3 Carrier Settling Time

This test was done using a real time spectrum analyzer. The analyzer has the capability to measure RF transients. This plot shows a settling time of approximately 200 µsecs.

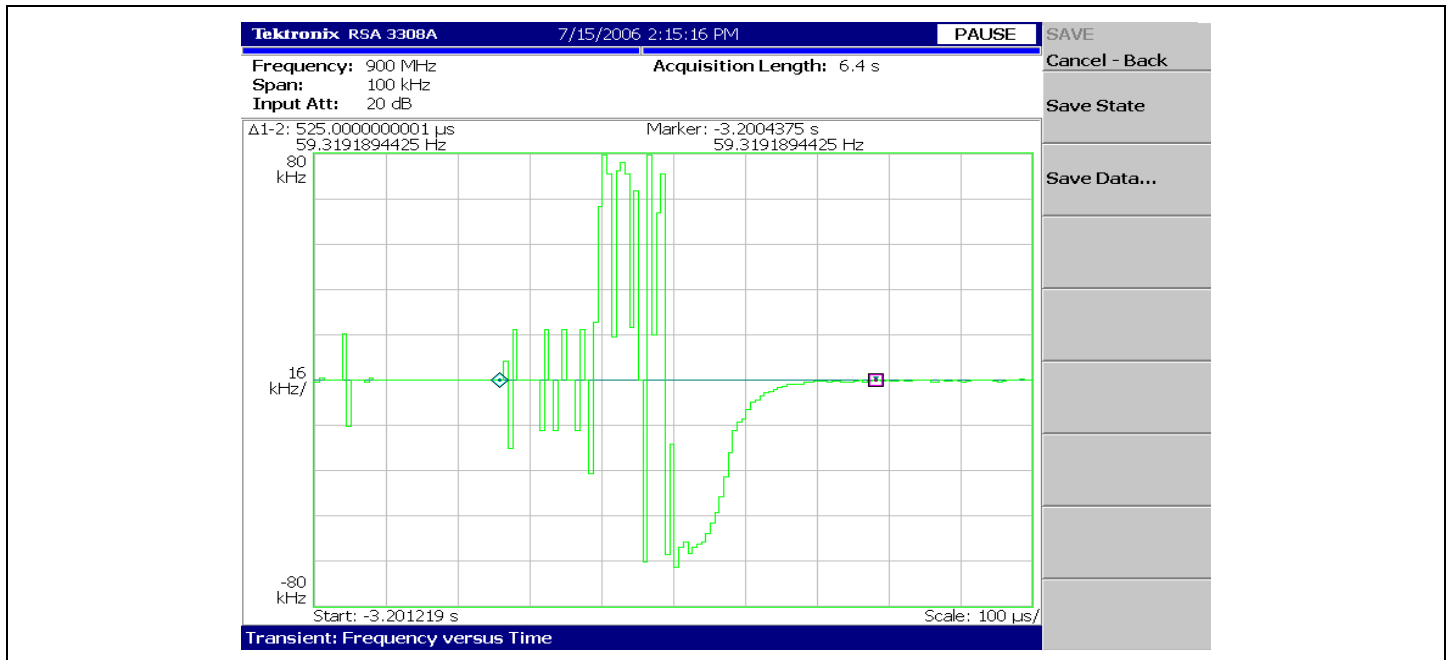


Figure 17: Carrier Settling Time

7.4 Rx Sensitivity Testing

FMO

The following data was taken on an A1 part. The method of testing Rx sensitivity is as follows:

- A random set of bits with a valid preamble is encoded in FM0. This pattern is sent through a DAC on an FPGA tag emulator test fixture. This DAC output drives the IF path on an external mixer. The LO port of this mixer is driven by an RF CW signal coming from the output of Indy R1000 reader chip. The output of the mixer now has a FM0 modulation at RF. The amplitude of this signal can easily be controlled with a step attenuator, thereby controlling the amplitude level at the Rx port of Indy R1000 reader chip. For each power level, 10k packets are sent and the packet error rate is computed; a packet error can occur if one bit is incorrect in a 128 bit packet. The setup details are given in the block diagram shown below. The same process is used for Miller 4 encoding.
- The external LO power level was set to 2 dBm. The board configuration has only a simple first order filter comprised of a series 100 nF cap. The measurements with the self-jammer are all taken in LNA low gain and DAC-bypass mode. An ESG 4426 was used to generate the CW interferer.

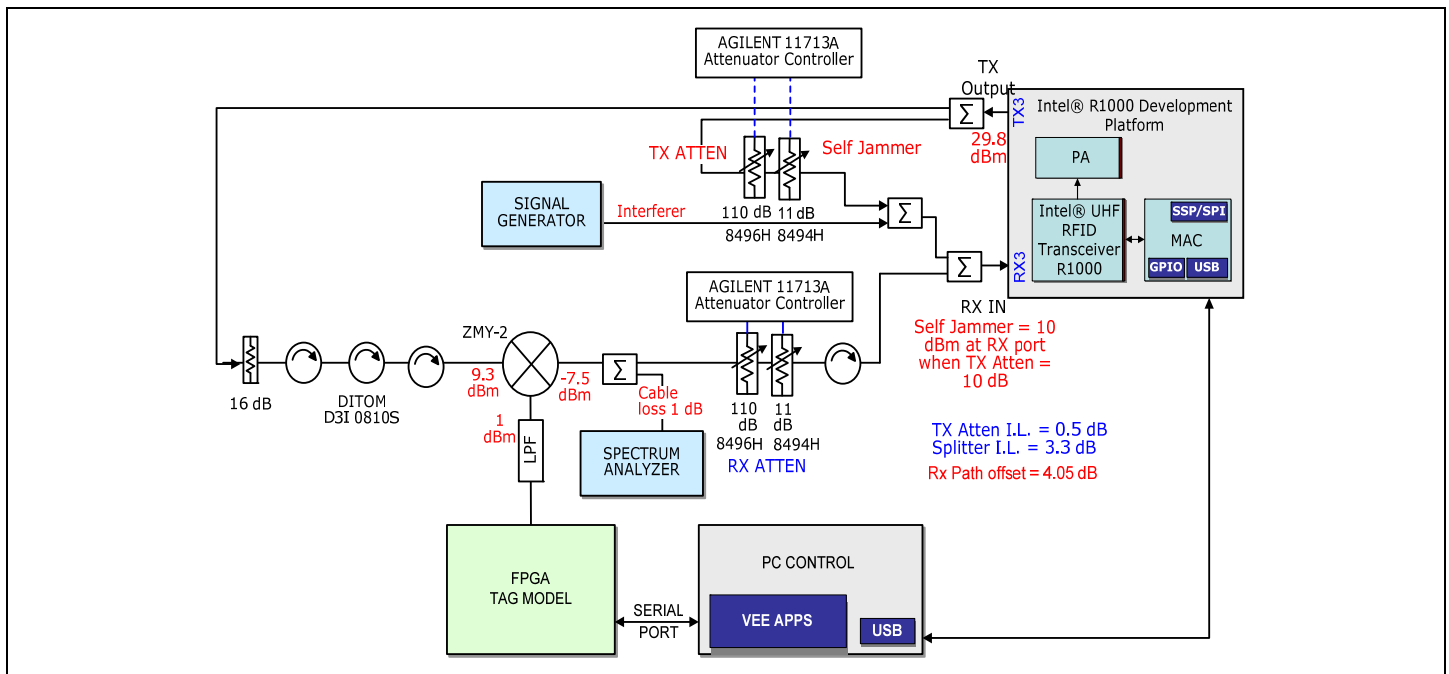


Figure 18: Packet Error Rate Test Setup - Monostatic Configuration

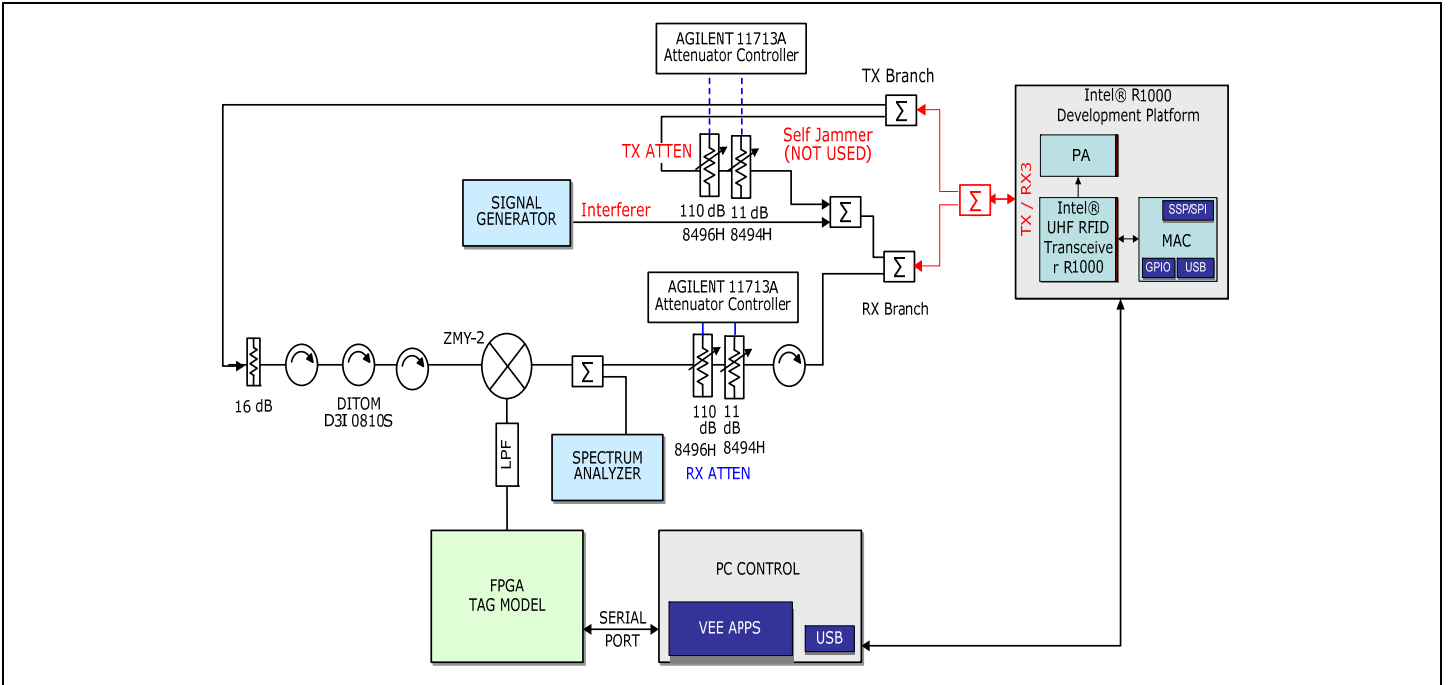


Figure 19: Packet Error Rate Test Setup - Bi-Static Configuration

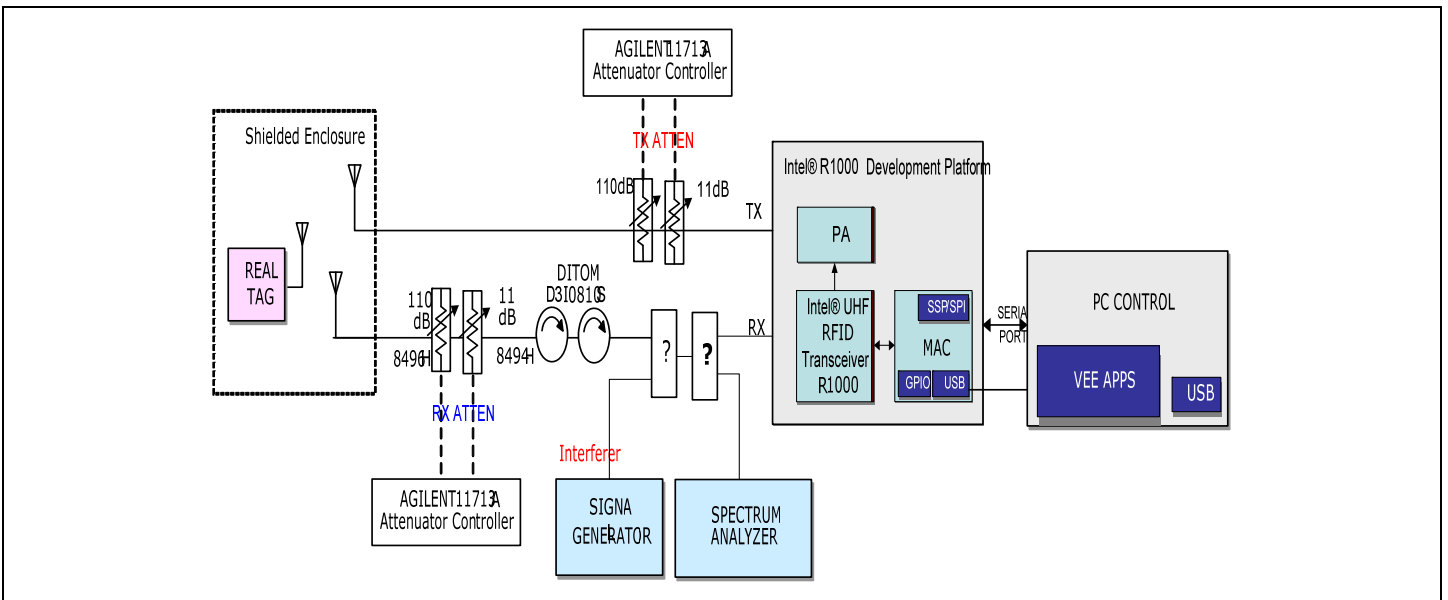


Figure 20: Packet Error Rate Test Setup - Real Tag

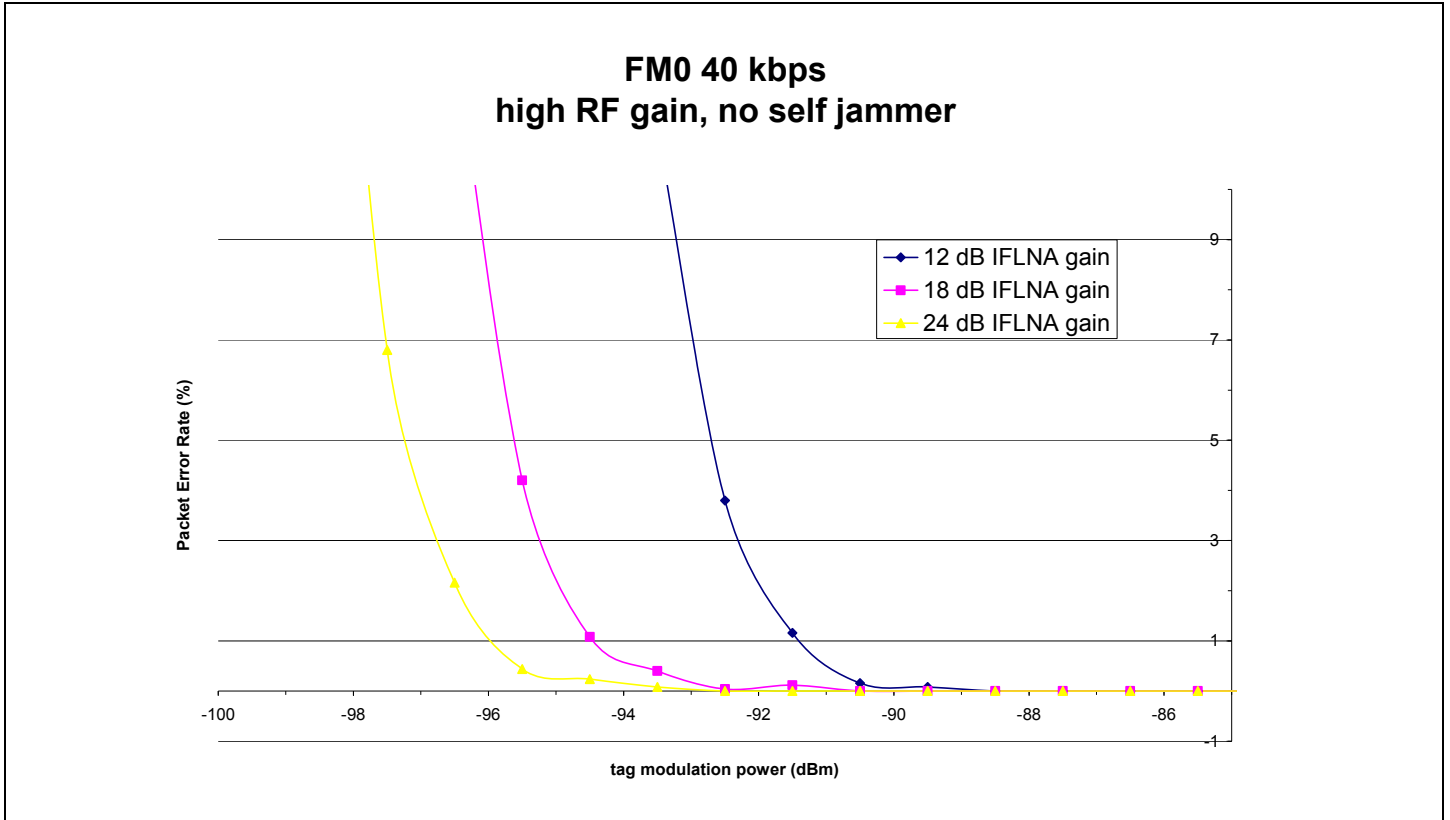


Figure 21: RX Sensitivity Plot: FM0, 40 kbps, No Self Jammer

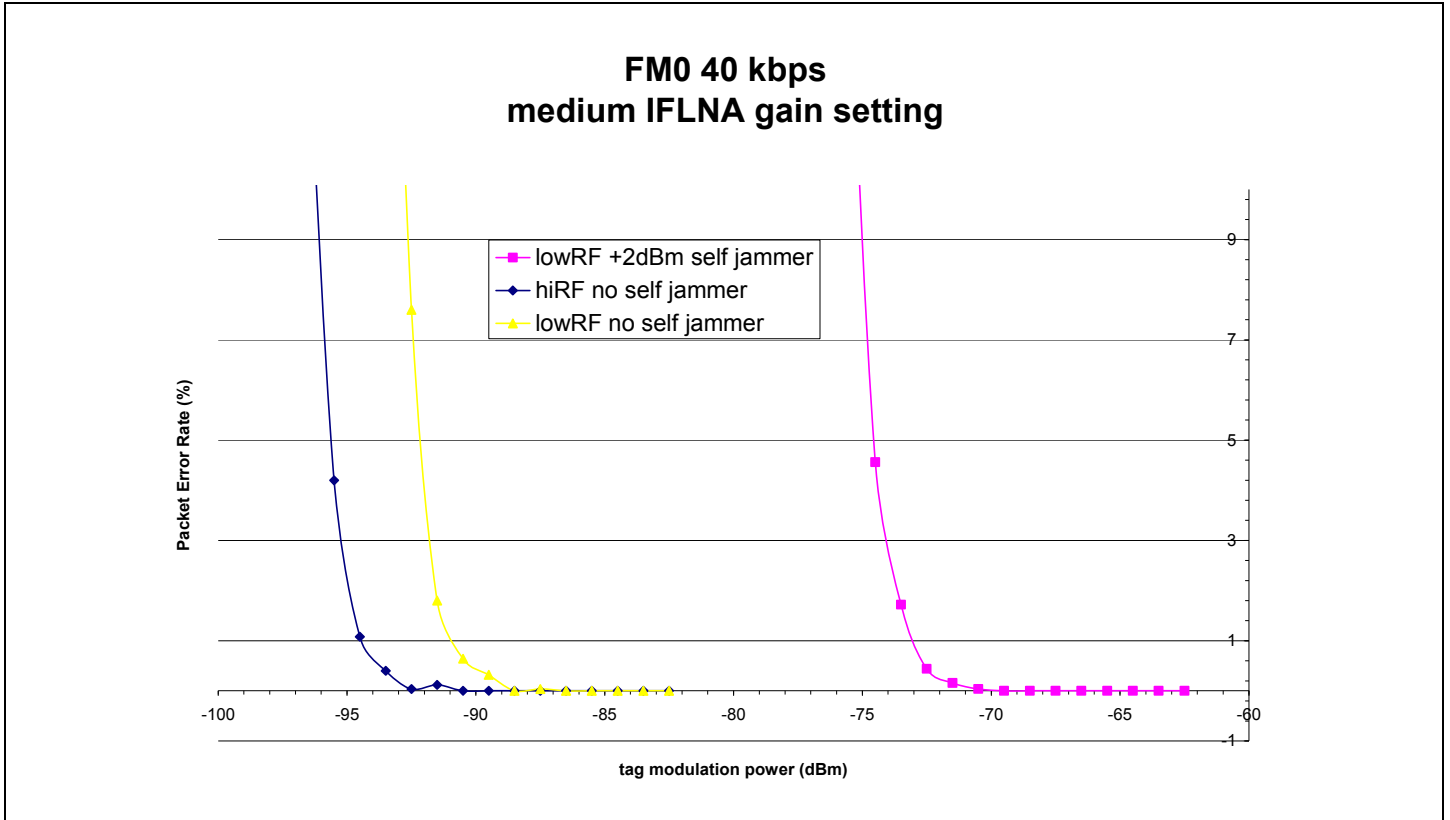


Figure 22: RX Sensitivity Plot: FM0, 40 kbps, Medium IFLNA Gain Setting

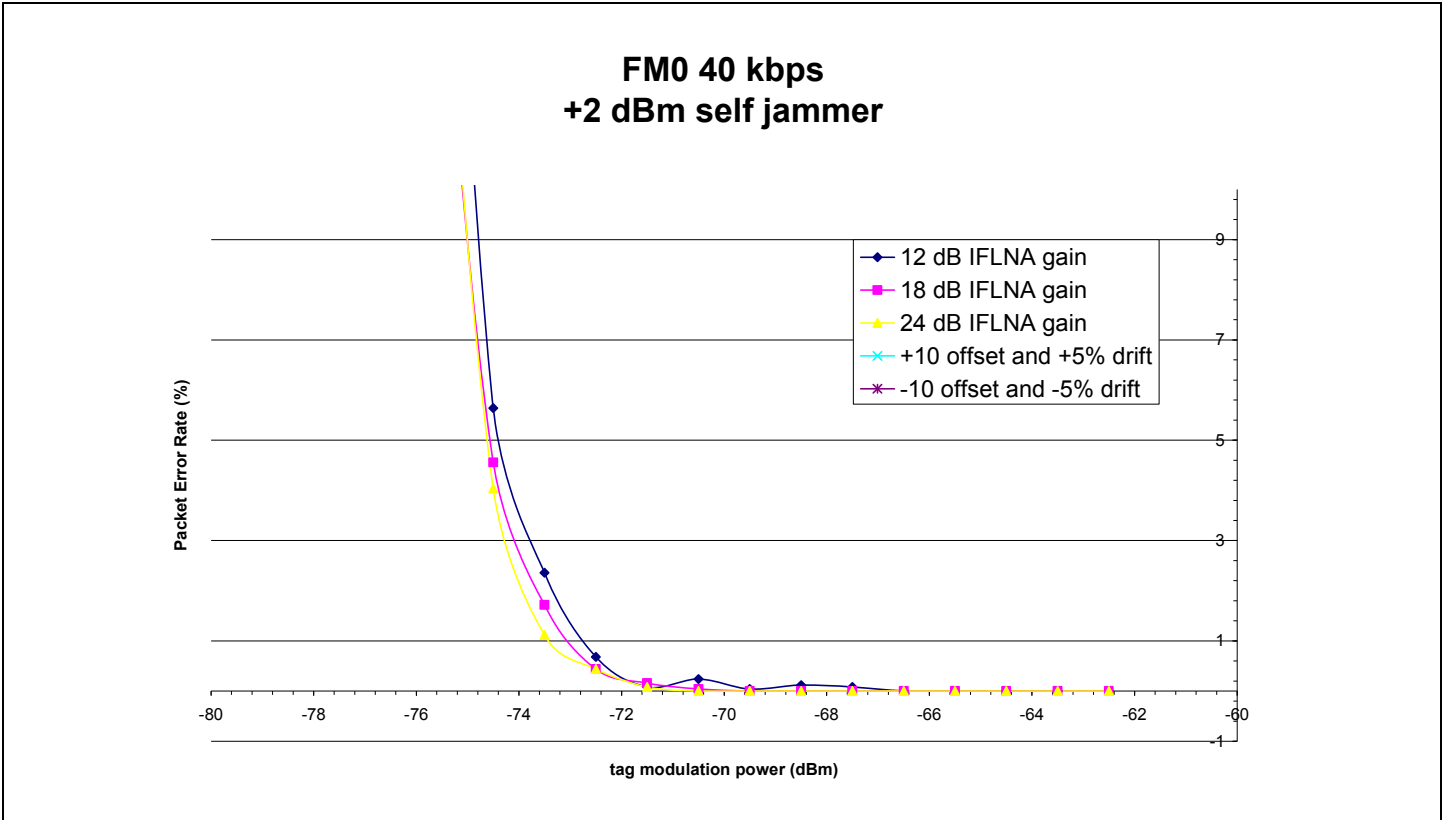


Figure 23: RX Sensitivity Plot: FM0, 40 kbps, +2 dBm, Self Jammer

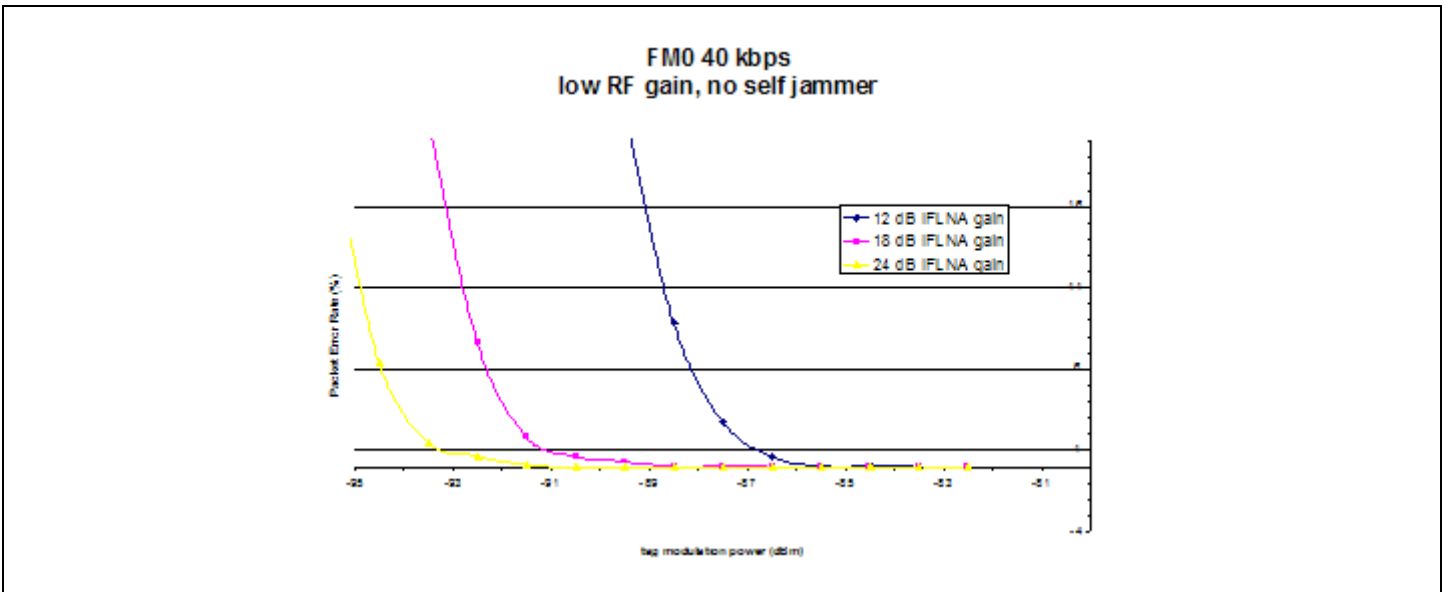


Figure 24: RX Sensitivity Plot: FM0, 40 kbps, Low RF Gain, No Self Jammer

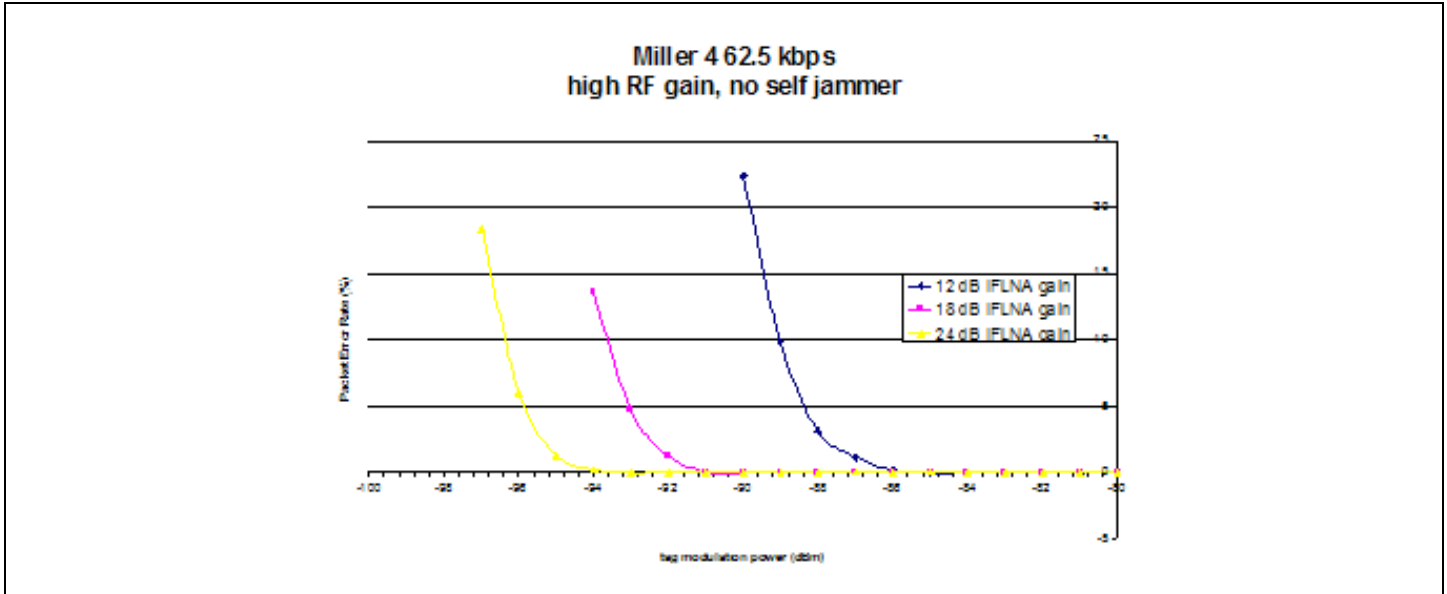


Figure 25: M4 62.5K (Dense Reader Mode)

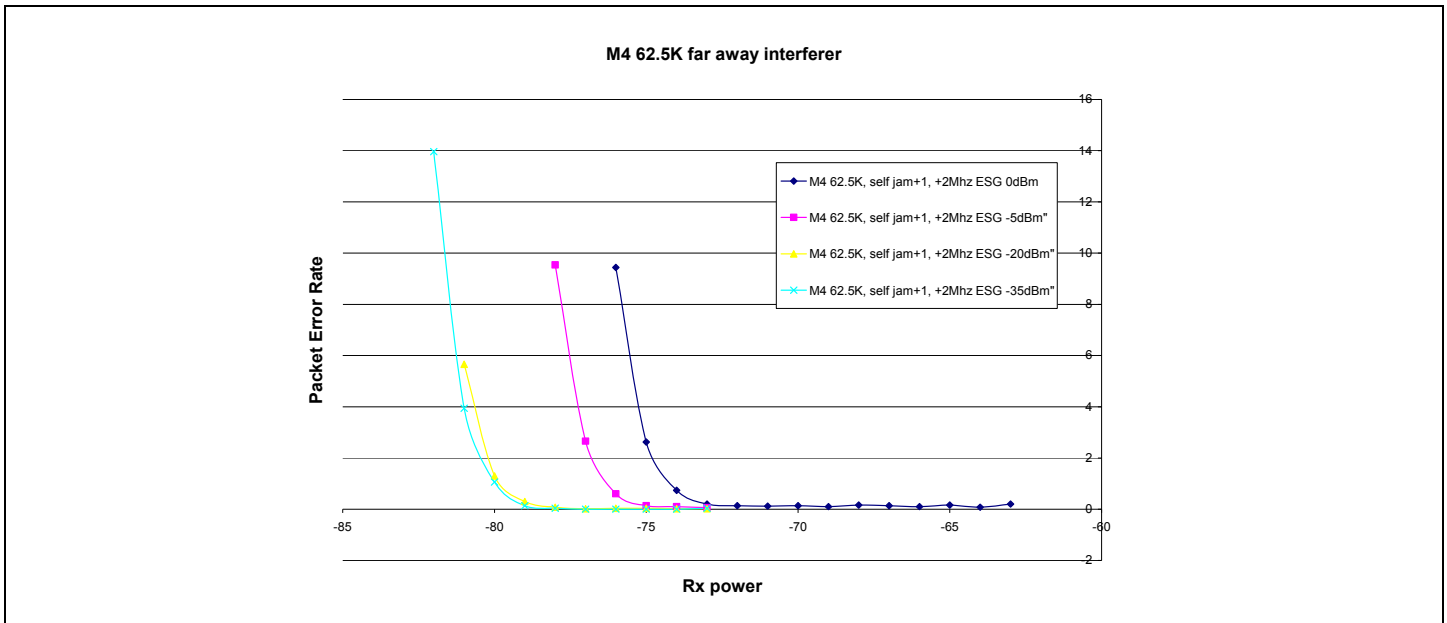


Figure 26: M4 62.5K Far Away Interferer

7.5 Transmit Output Spectral Testing

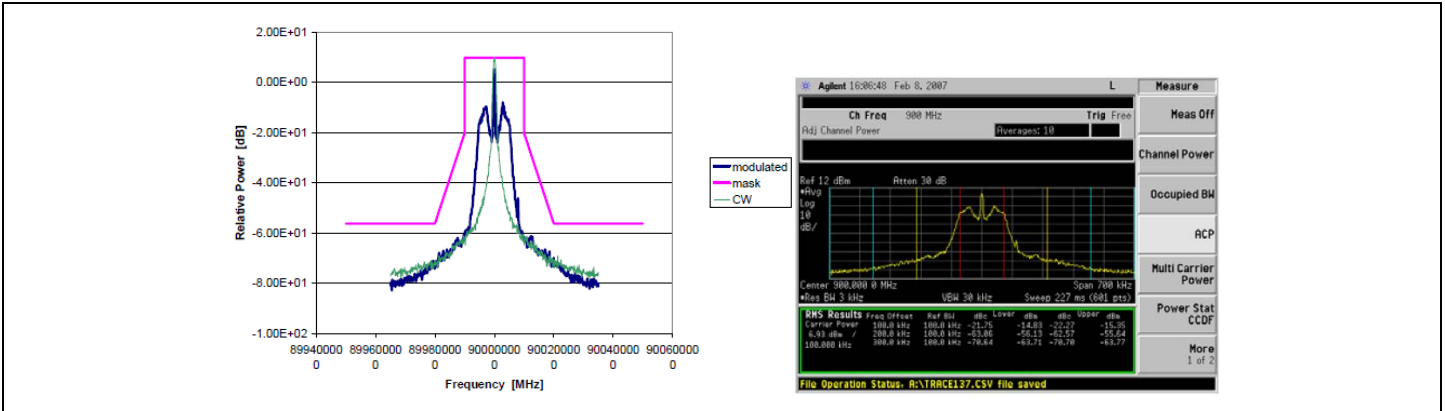


Figure 27: Indy R1000 Reader Chip Transmit Modulation and Mask for DSB, Tari=25 μsec, X=0.5

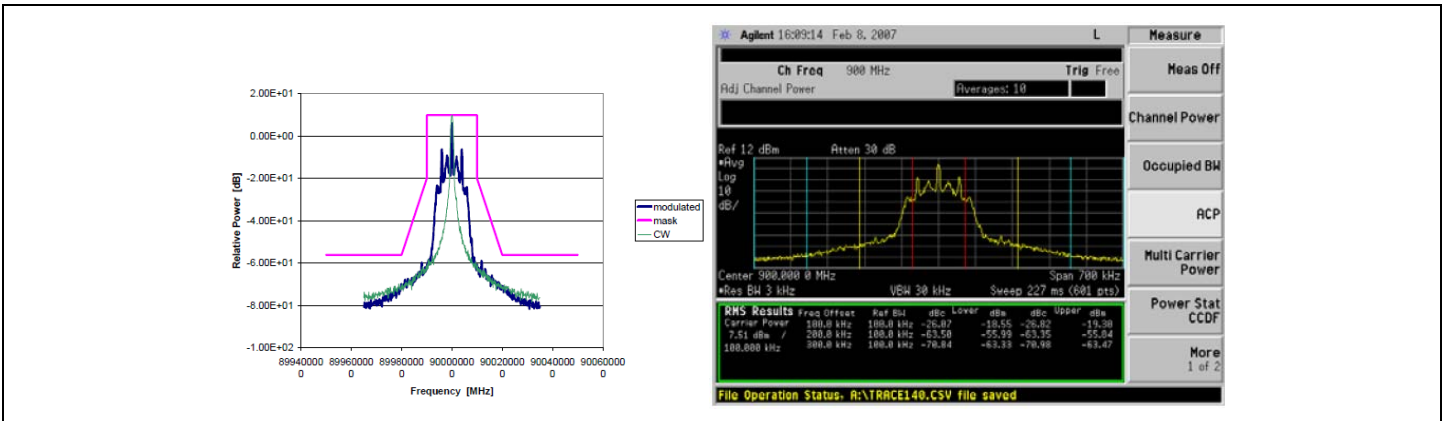


Figure 28: Indy R1000 Reader Chip Transmit Modulation and Mask for DSB, Tari=25 μsec, X=1

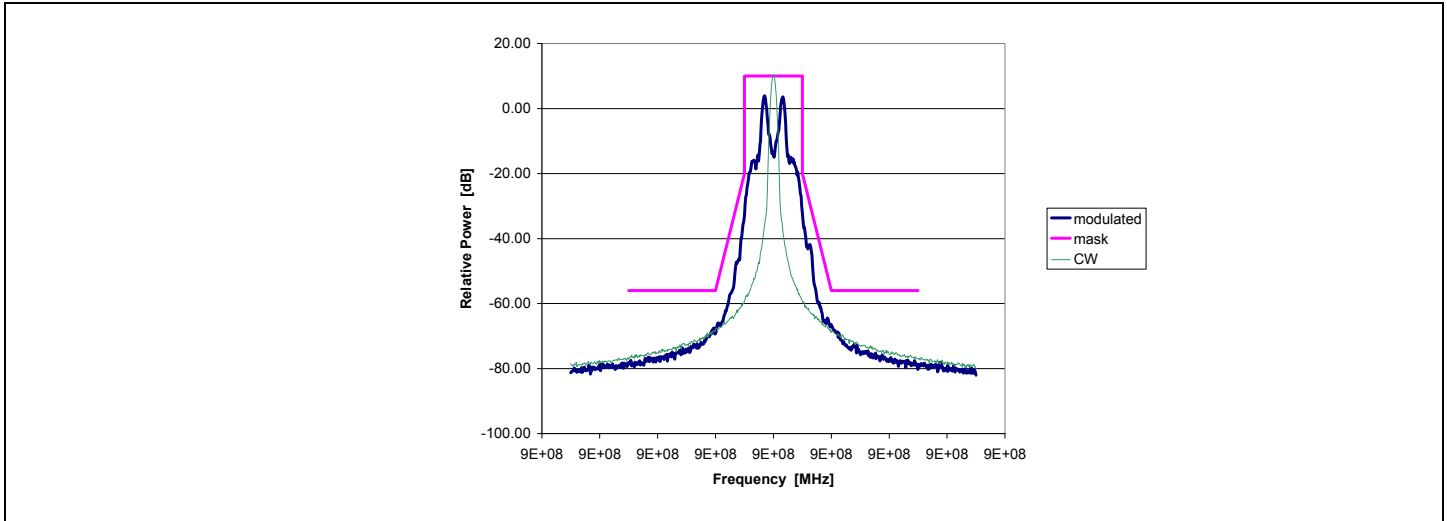


Figure 29: Indy R1000 Reader Chip Transmit Modulation and Mask for PR-ASK, $T_{\text{ari}}=12.5 \mu\text{sec}$, $X=0.5$

Note: The limit lines include a 6 dB margin at 200 KHz.

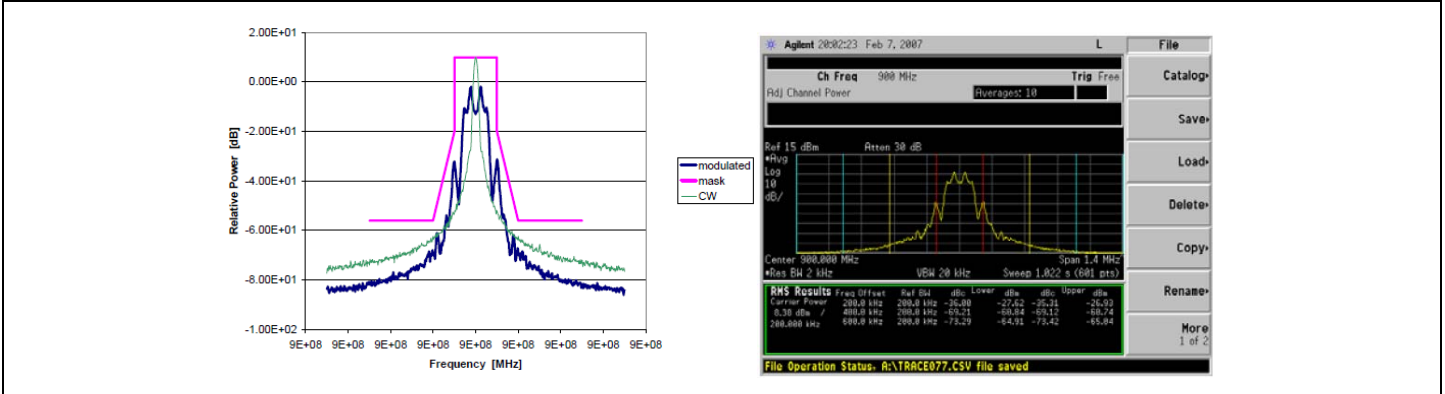


Figure 30: Indy R1000 Reader Chip Transmit Modulation and Mask for PR-ASK, Tari=12.5 μsec, X=1

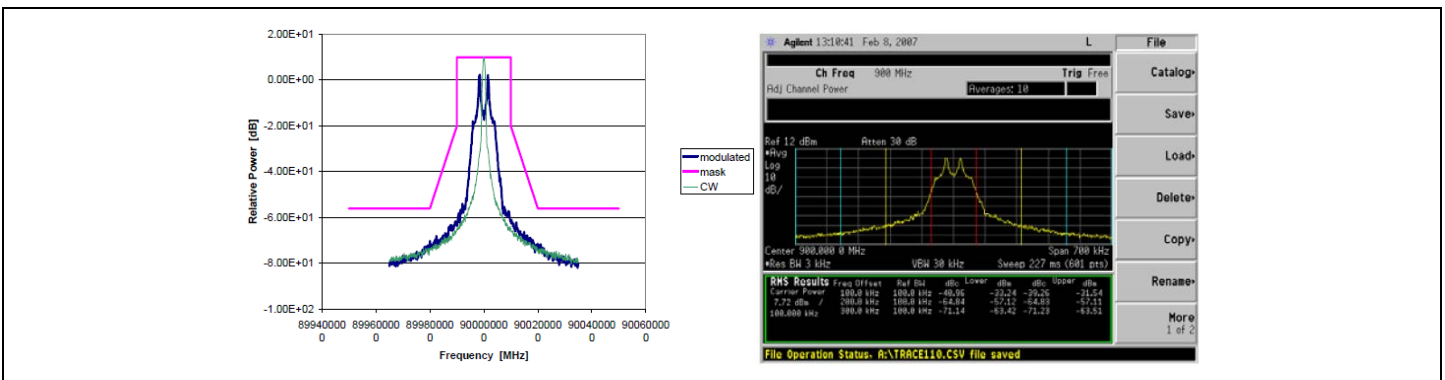


Figure 31: Indy R1000 Reader Chip Transmit Modulation and Mask for PR-ASK, Tari=25 μsec, X=0.5

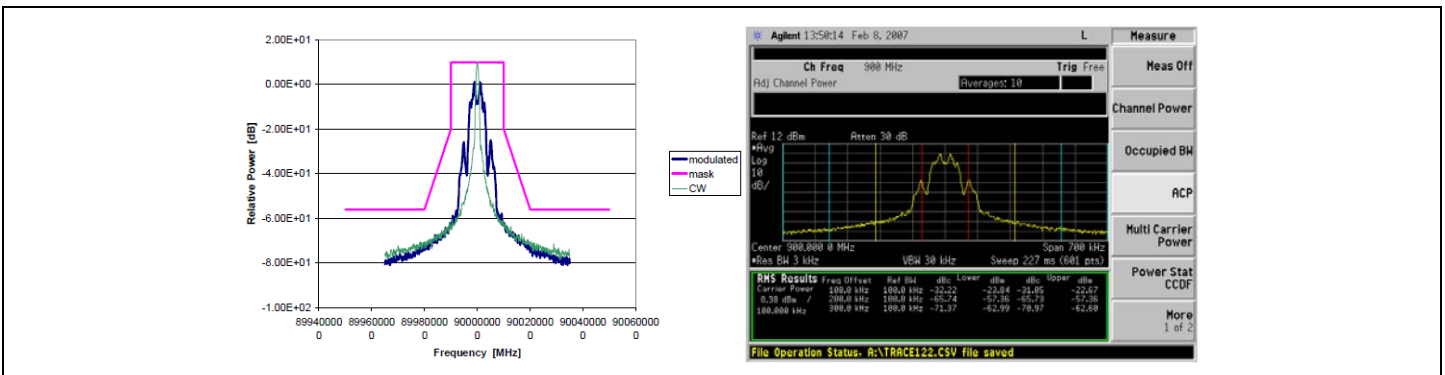


Figure 32: Indy R1000 Reader Chip Transmit Modulation and Mask for PR-ASK, Taro= 25 μsec, X=1

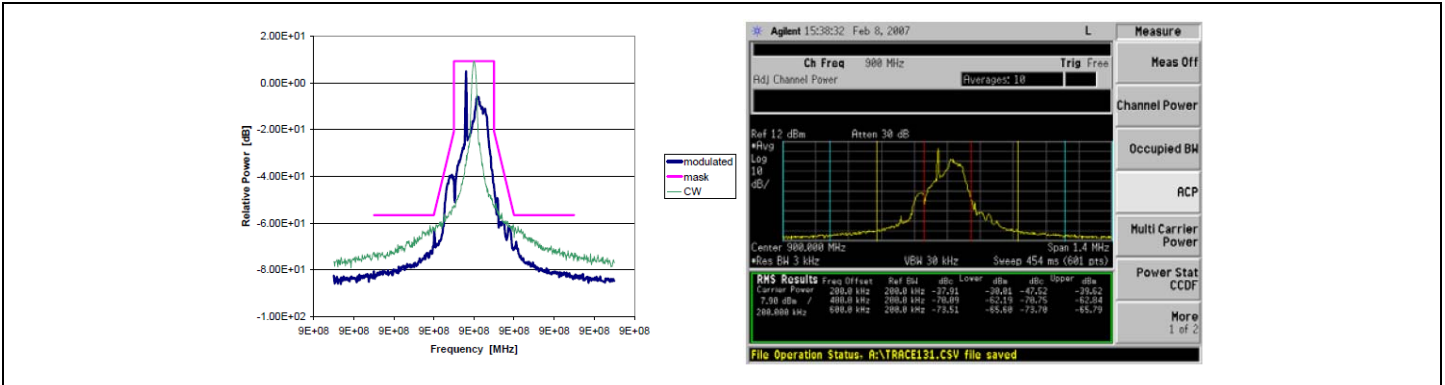


Figure 33: Indy R1000 Reader Chip Transmit Modulation and Mask for SSB, Tari=12.5 μsec, X=0.5

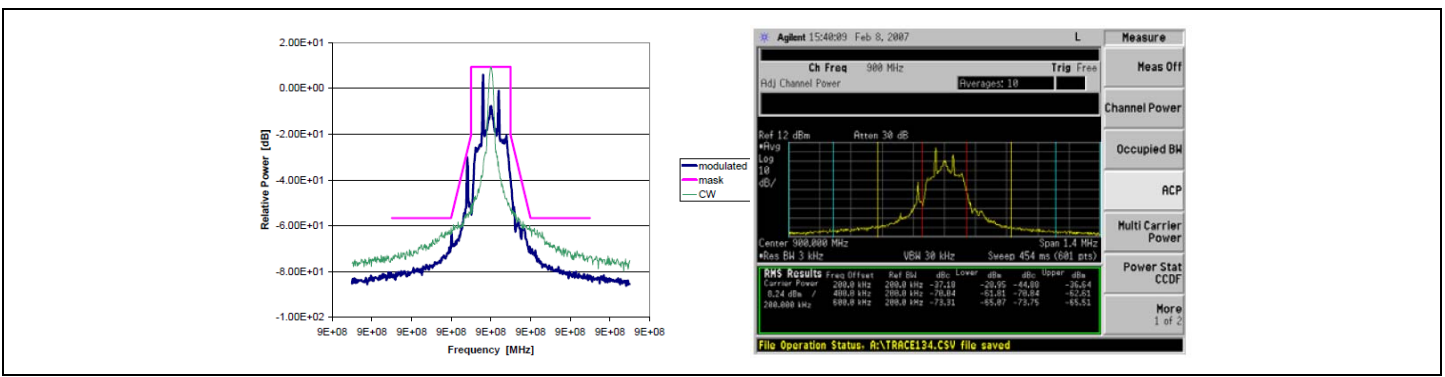


Figure 34: Indy R1000 Reader Chip Transmit Modulation and Mask for SSB, Tari=12.5 μsec, X=1

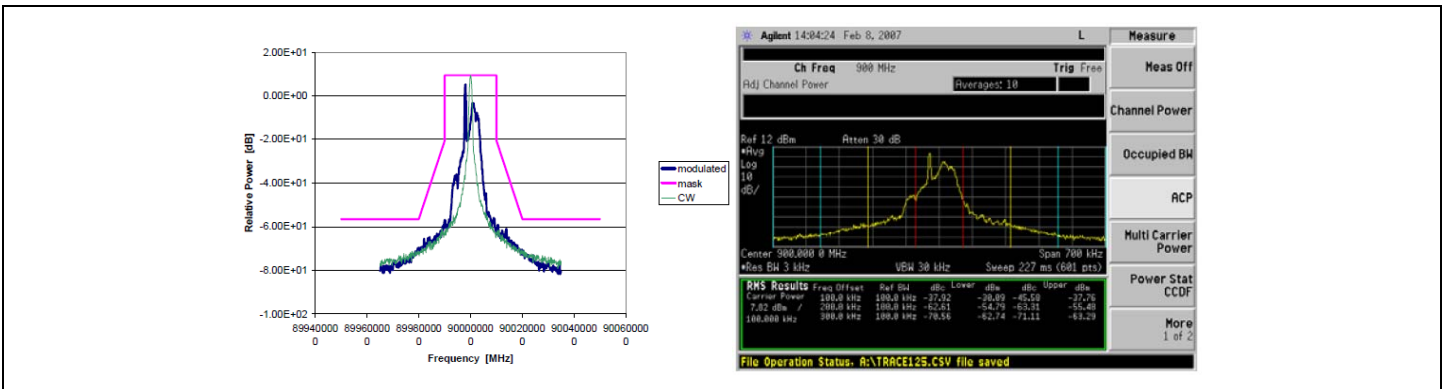


Figure 35: Indy R1000 Reader Chip Transmit Modulation and Mask for SSB, Tari=25 μsec, X=0.5



Figure 36: Indy R1000 Reader Chip Transmit Modulation and Mask for SSB, Tari=25 μsec, X=1

7.6 Gain Control Resolution and Dynamic Range

| | |
|---------------------------|---------|
| Board N2 | Chip296 |
| 6 dB pad at PA O/P | |
| Spectrum Analyzer setting | |
| RB | 3 KHz |
| VRB | 300 Hz |
| Detector | RMZ |

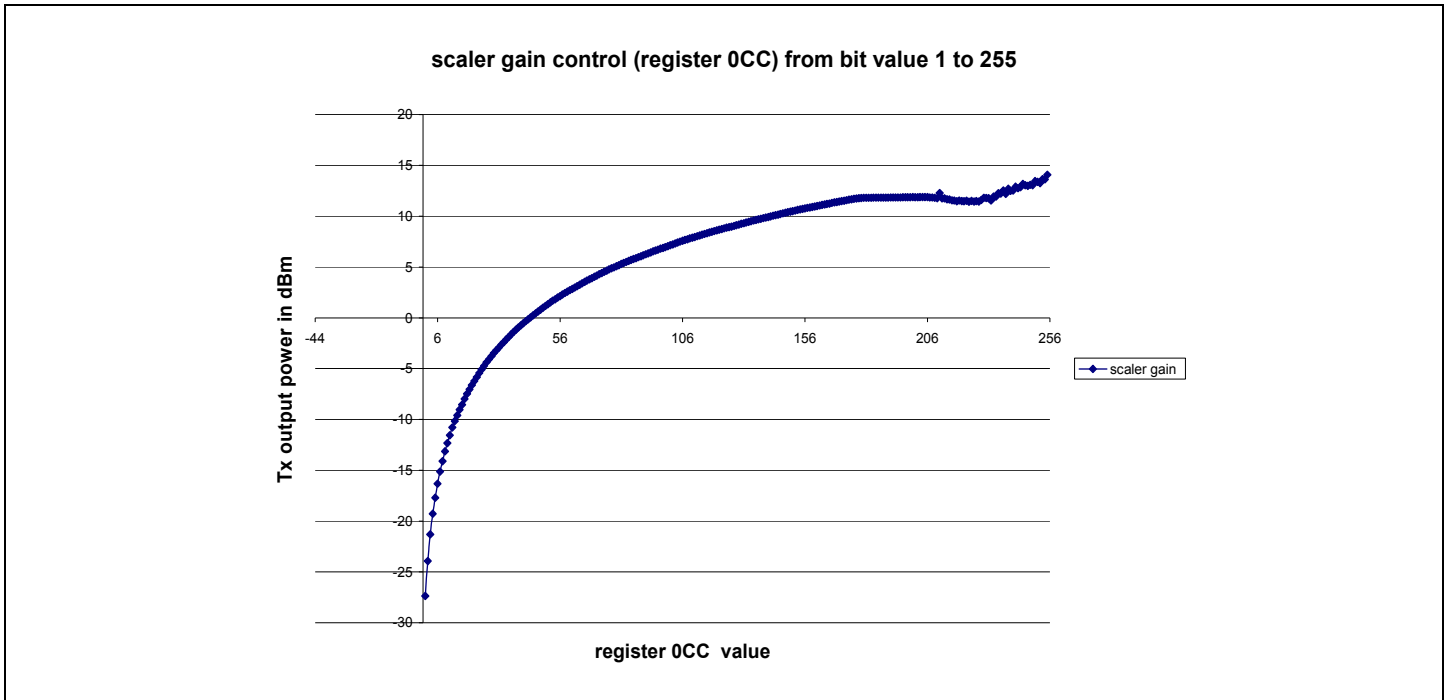


Figure 37: Tx Output Power Scaler Gain Control

Table 25: Mixer Gain Settings

| Reg: 414 | Reading | PA O/P at 900 MHz (dBm) | Gain (dB) |
|----------|---------------|-------------------------|-----------|
| | 0dda (-10 dB) | 3.02 | |
| | 0dc2 (-12 dB) | 0.85 | -2.17 |
| | 0d9a (-18 dB) | -5.05 | -8.07 |
| | 0d92 (-20 dB) | -6.96 | -9.98 |

Table 26: PA Power Gain Settings

| Reg: 415 | Reading | Power at 900 MHz (dBm) | Gain (dB) |
|----------|--------------|------------------------|-----------|
| | 1efd (17 dB) | 3.8 | |
| | 1e1d (13 dB) | 0.5 | -3.3 |

7.7 ADC Testing

The plot in Figure 38 shows the static performance of the Aux. ADC performance. Board N2 was used for this testing. Register 284 is used to select the channel; register 10D was read as the output. This test was done using a step size of 50 mV; we need to improve this resolution to 1mV in order to make useful INL and DNL calculations. We may use a 14-bit DAC for future measurements.

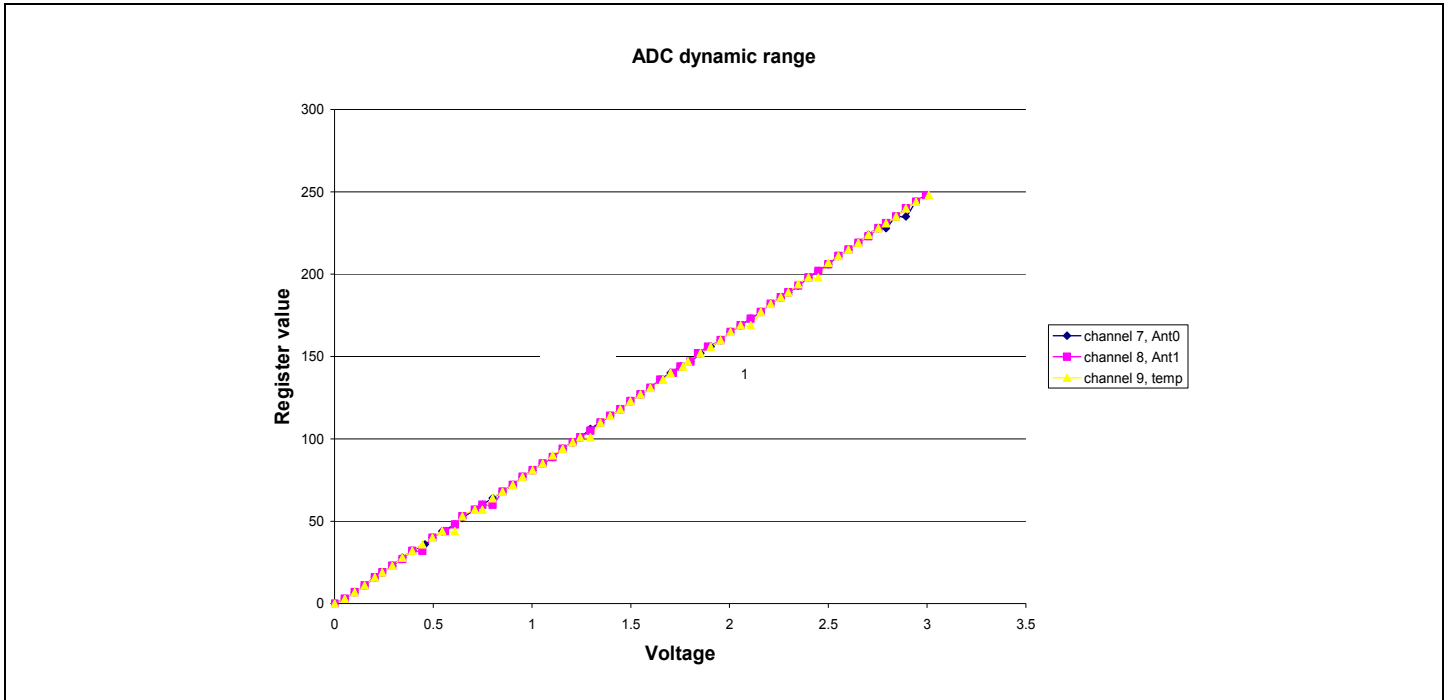


Figure 38: ADC Dynamic Range and Linearity

7.8 Aux. DAC Testing

The plots in [Figure 39](#), [Figure 39](#): DAC Linearity and Range

, and [Figure 41](#) show the static performance of the PA bias and PA regulator DAC performance. Board N2 was used for this test. A multi-meter was used to make the DAC output measurements. $V_{lsb} = 3/256 = 0.11718V$.

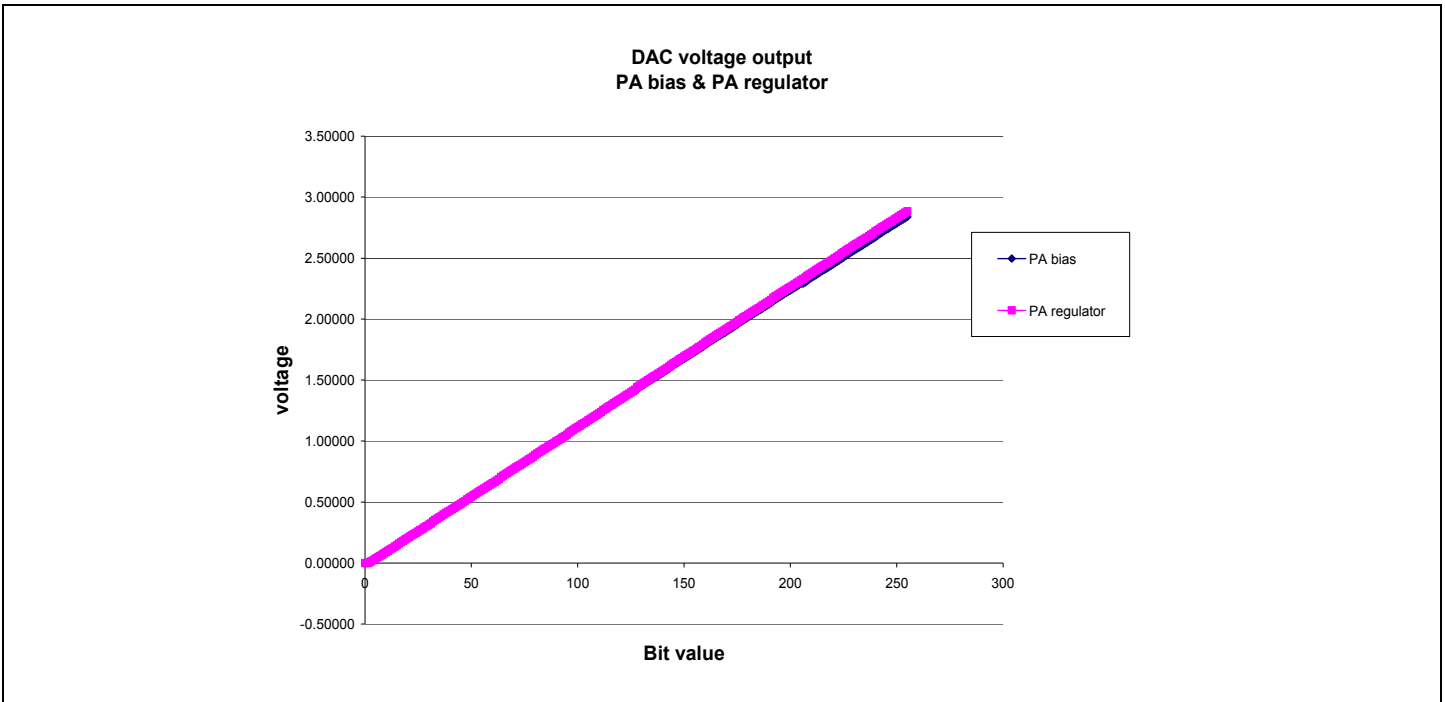


Figure 39: DAC Linearity and Range

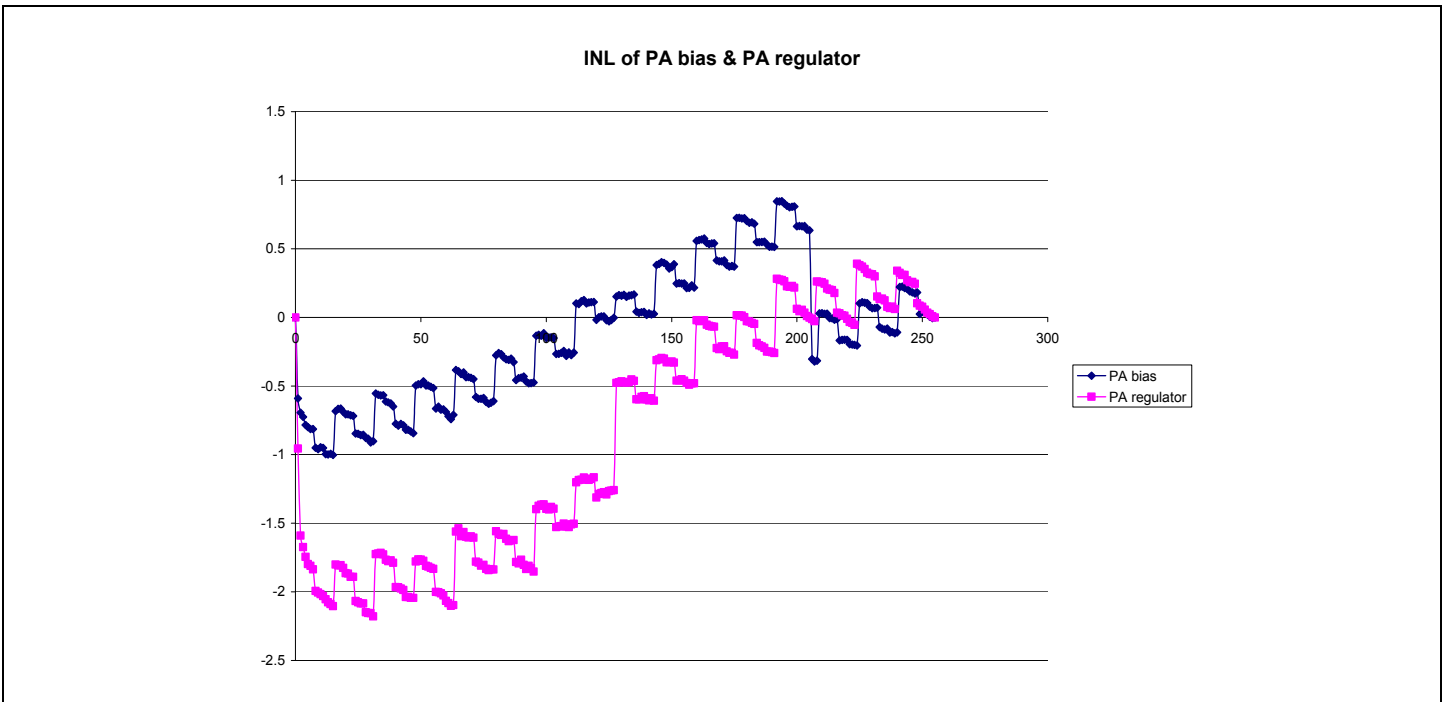


Figure 40: Integral Non-Linearity of PA Bias and PA Regulator DACs

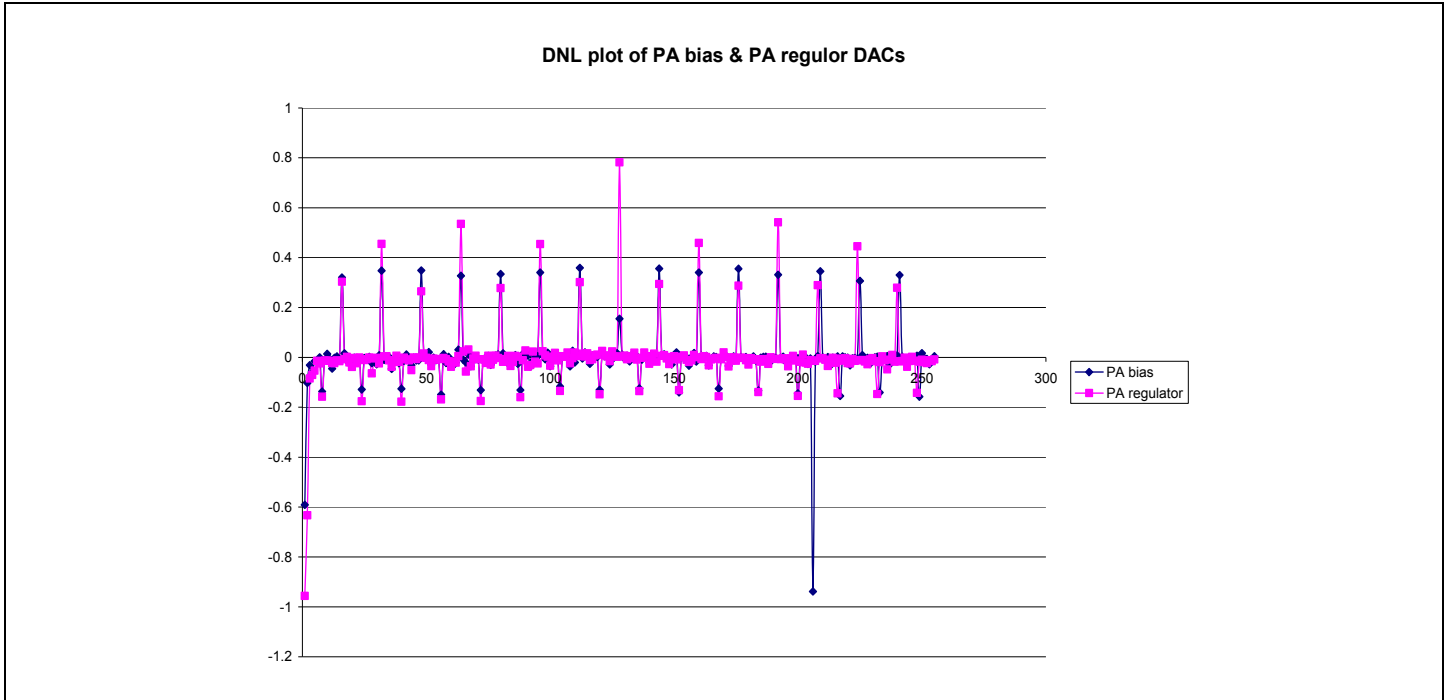
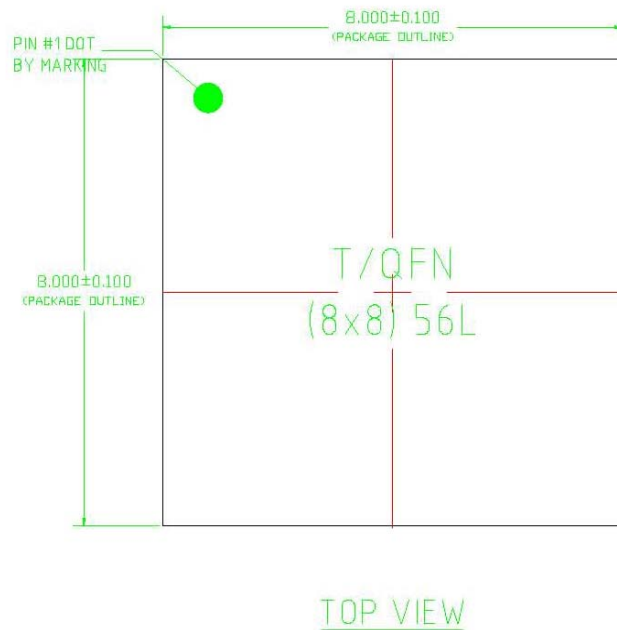


Figure 41: Differential Non-Linearity of PA Bias and PA Regulator DACs

8 Package Information

8.1 Package Information

The Indy R1000 reader chip RFID Radio chip is packaged in a 56 pin, 8 mm x 8 mm x 1 mm, 0.50 mm pitch, quad flat no-lead (QFN) package. [Figure 42](#) and [Figure 43](#) provide top views of the Indy R1000 reader chip package, and [Figure 44](#) provides the bottom and side views.



NOTES:

1. ALL DIMENSIONS ARE IN MM UNLESS OTHERWISE SPECIFIED.
2. QFN AND TQFN SHARE THE EXPOSE OUTLINE BUT WITH DIFFERENT THICKNESS.

| | | QFN | TQFN |
|---|------|-------|-------|
| A | MAX. | 1.000 | 0.800 |
| | NOM. | 0.850 | 0.750 |
| | MIN. | 0.800 | 0.700 |

Figure 42: Indy R1000 Reader Chip Package Top View

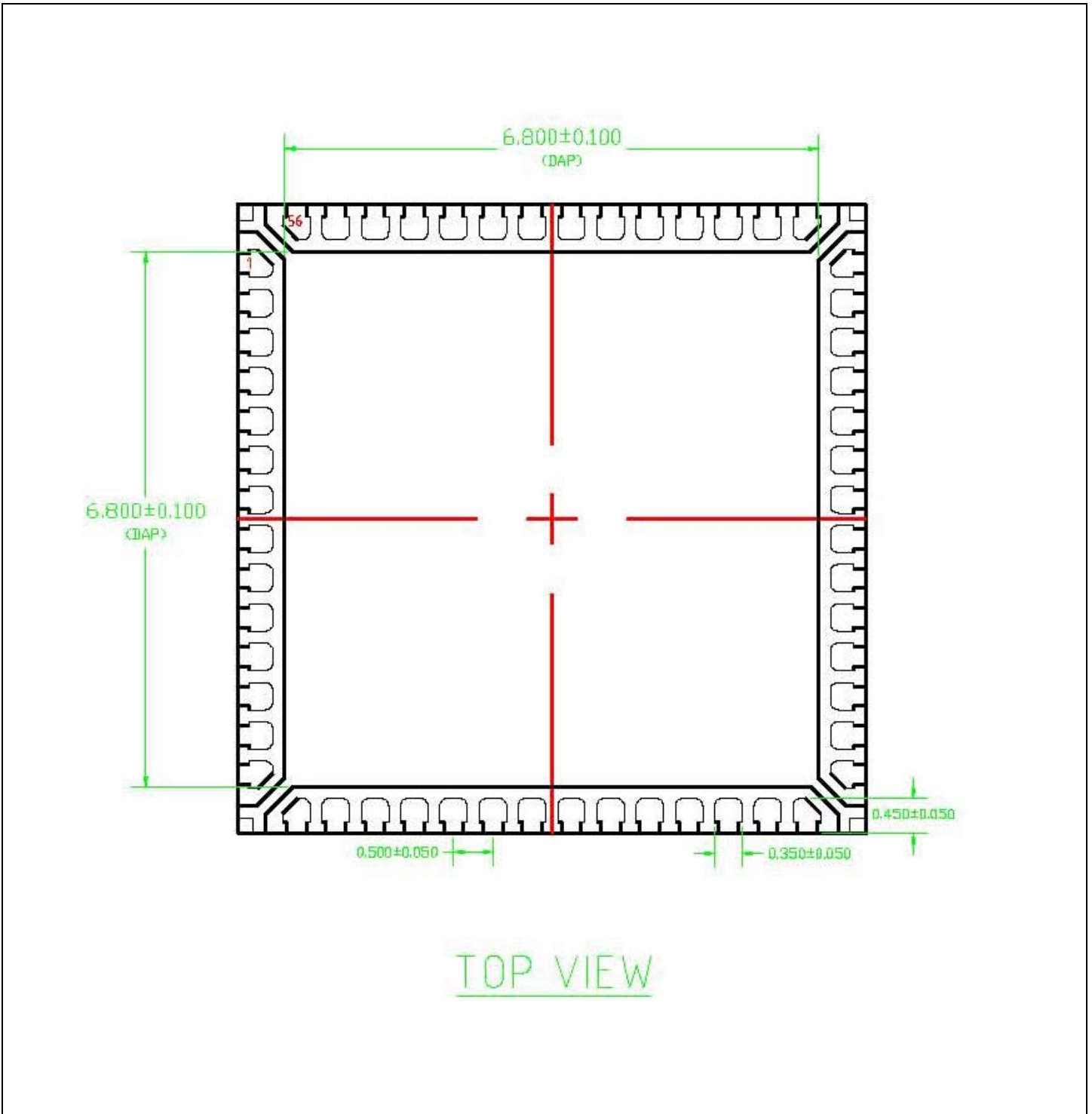


Figure 43: Indy R1000 Reader Chip Package Top View

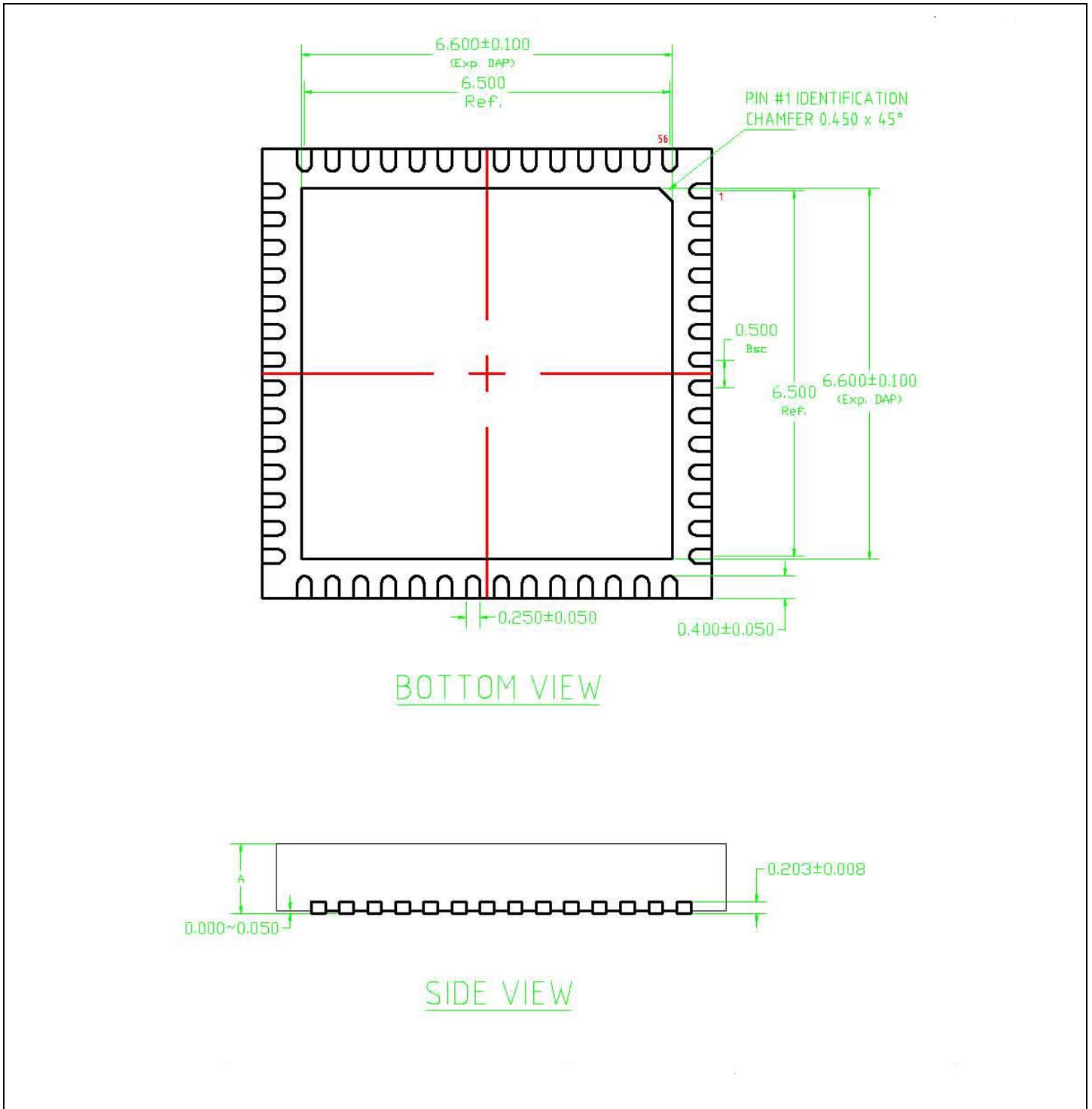
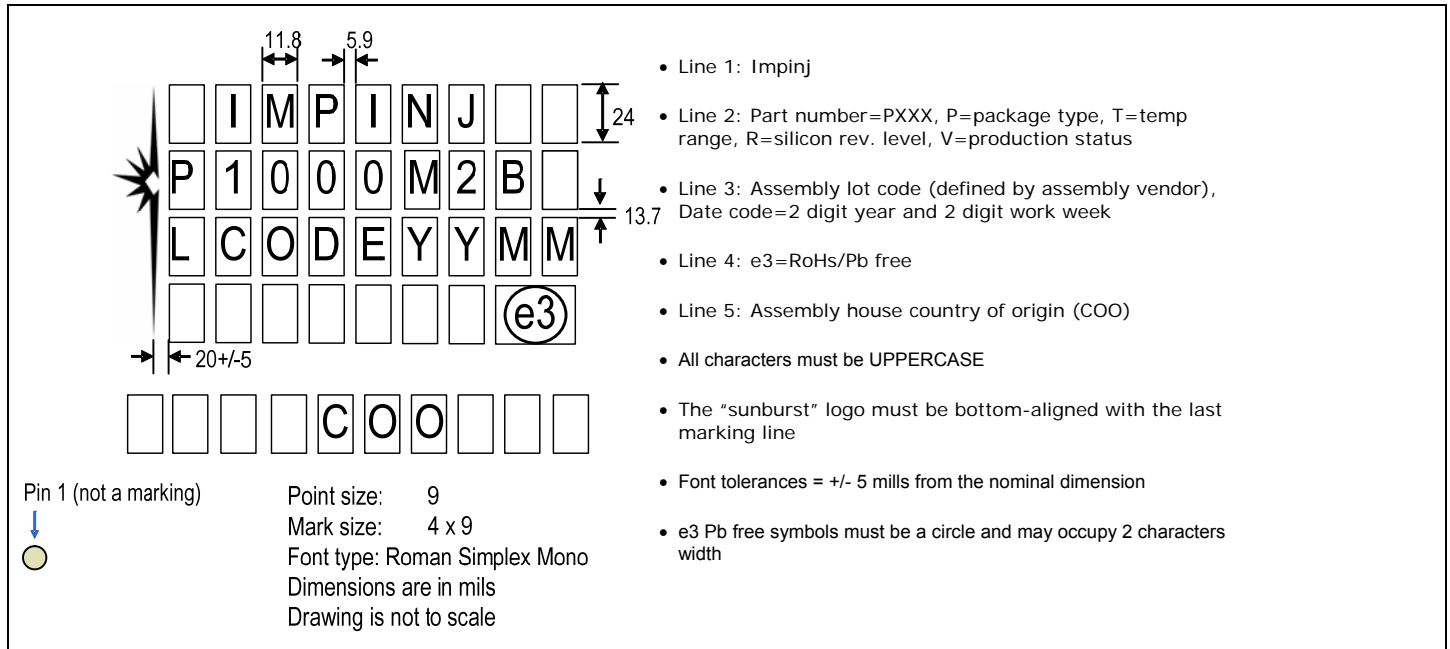


Figure 44: Indy R1000 Reader Chip Package Bottom and Side Views

8.2 Package Markings

The diagram in this section details the package top markings, which identify the Indy R1000 reader chip in the 56-pin QFN package.





Notices:

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